19-4348; Rev 0; 10/08

EVALUATION KIT AVAILABLE

Internal-Switch Boost Regulator with Integrated 7-Channel Driver, VCOM Calibrator, Op Amp, and LDO

General Description

The MAX17094 includes a high-performance step-up regulator, a 250mA low-dropout (LDO) linear regulator, a high-speed operational amplifier, a digitally adjustable VCOM calibration device with nonvolatile memory and I²C interface, and seven integrated high-voltage level shifters. The device is optimized for thin-film transistor (TFT) liquid-crystal display (LCD) applications.

The step-up DC-DC converter is a current-mode regulator that provides the regulated supply voltage for panel source driver ICs. The current-mode architecture provides fast-transient responses to pulsed loads typical of source driver loads. The high switching frequency, which is programmable to any frequency between 450kHz to 1.2MHz with a single resistor, allows the use of ultra-small inductors and ceramic capacitors. The step-up regulator's soft-start time is controlled by an internal 10ms digital timer that requires no external components; or if desired, the soft-start time can be adjusted by adding a single external capacitor.

The low-voltage LDO linear regulator can provide at least 250mA. The output voltage is accurate within ±2%.

The high-voltage, level-shifting scan driver is designed to work with panels that incorporate row drivers on the panel glass. Its seven outputs swing from +30V to -10V and can swiftly drive capacitive loads.

The high-performance op amp is designed to drive the LCD backplane and features 20MHz bandwidth, 45V/µs slew rate, and 150mA output currents.

The programmable VCOM calibrator is externally attached to the VCOM amplifier's resistive voltage-divider and sinks a programmable current to adjust the VCOM voltage level. An internal 7-bit digital-to-analog converter (DAC) controls the sink current. The DAC is ratiometric relative to AVDD and is guaranteed monotonic over all operating conditions. The calibrator includes a nonvolatile memory device (IVR) to store the desired VCOM voltage level. The 2-wire I²C interface simplifies production equipment.

The MAX17094 is available in a 48-pin, 6mm x 6mm TQFN package with a maximum thickness of 0.8mm for thin LCD panels.

Applications

Notebook Computer Displays

Features

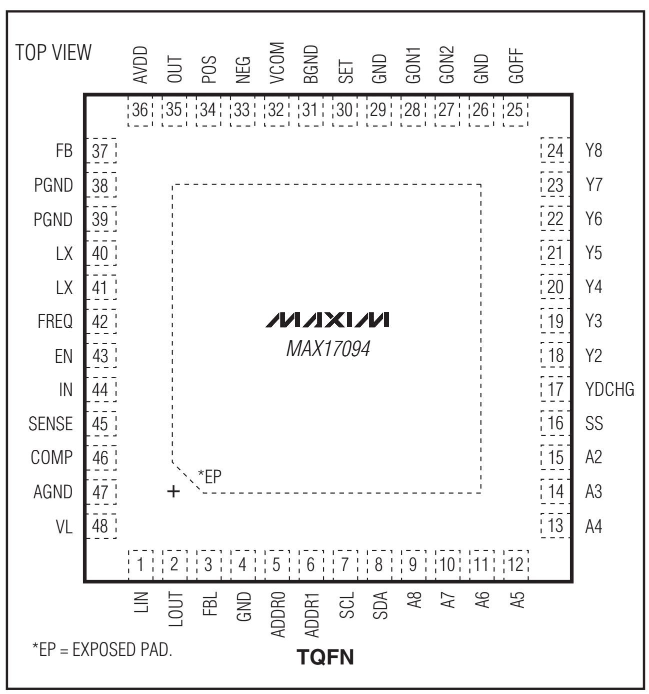
- **1.8V to 5.5V IN Supply Voltage Range**
- **450kHz to 1.2MHz Adjustable Frequency Current-Mode Step-Up Regulator**
  - **Fast-Transient Response**
  - **Integrated 14V, 2.5A, 150mΩ MOSFET**
  - **High Efficiency (> 85%)**
- **Low-Dropout Linear Regulator**
  - **High-Accuracy Output Voltage (2.0%)**
  - **Internal Digital Soft-Start**
- **High-Performance Operational Amplifier**
  - **200mA Output Short-Circuit Current**
  - **45V/µs Slew Rate**
  - **20MHz, -3dB Bandwidth**
  - **Rail-to-Rail Inputs and Outputs**
- **High-Voltage Drivers**
  - **+30V to -10V Outputs**
- **I²C Programmable VCOM Calibrator**
  - **7-Bit Adjustable Current-Sink Output**
  - **Nonvolatile IVR Memory**
- **Thermal-Overload Protection**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17094ETM+	-40°C to +85°C	48 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration



ABSOLUTE MAXIMUM RATINGS

IN, LIN, LOUT, EN, VL, A2–A8,
SCL, SDA, ADDR0, ADDR1.............................-0.3V to +7.5V
COMP, FB, SENSE, SS to AGND...............-0.3V to (V_{VL} + 0.3V)
FBL to AGND..-0.3V to (V_{LIN} + 0.3V)
FREQ, SET to GND....................................-0.3V to (V_{VL} + 0.3V)
LX to PGND...-0.3V to +16V
AVDD to BGND...-0.3V to +16V
POS, NEG, OUT, VCOM to BGND ......-0.3V to (V_{AVDD} to +0.3V)
POS to NEG..-6V to +6V
GND, PGND, BGND to AGND...............................-0.3V to +0.3V
GON1, GON2 to GND ....-0.3V to +35V
GOFF to GND...-14V to + 0.3V
Y2–Y6, YDCHG to GND ....(V_{GOFF} - 0.3V) to (V_{GON1} + 0.3V)
Y7, Y8 to GND.........................(V_{GOFF} - 0.3V) to (V_{GON2} + 0.3V)
LX, PGND RMS Current 2.4A
Y1–Y7, YDCHG RMS Current...33mA
GON1 RMS Current 46mA
GON2 RMS Current 83mA
GOFF RMS Current 115mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin, 6mm x 6mm TQFN
(derate 20mW/°C above +70°C).. ....2963mW
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{LIN} = V_{EN} = +3.3V, circuit of Figure 2, V_{MAIN} = 8V, V_{GON1} = V_{GON2} = 21V, V_{GOFF} = -6.5V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
IN Input-Voltage Range		1.8		5.5	V
IN Shutdown Current	EN = 0		30	100	µA
IN Quiescent	V_{IN} = 3V, V_{FB} = 1.5V, not switching, V_L > 2.3V			100	µA
IN Undervoltage Lockout	V_{IN} rising, typical hysteresis 200mV		1.30	1.75	V
Thermal Shutdown	Rising edge, typical hysteresis 15°C		160		°C
BOOTSTRAP LINEAR REGULATOR (VL)					
VL Output Voltage		3.8	4.0	4.2	V
VL Maximum Output Current	VL = 3.7V	10			mA
LINEAR REGULATOR					
LIN Input-Voltage Range	V_{LOUT} < V_{LIN}	1.8		5.5	V
LIN Quiescent Current	No load			2	mA
Dropout Voltage	I_{LOUT} = 250mA, V_{LIN} - V_{LOUT}			0.3	V
FBL Regulation Voltage	I_{LOUT} = 100mA	605	618	631	mV
FBL Input Bias Current	V_{FBL} = 0.618V, T_A = +25°C	-50		+50	nA
LOUT Maximum Output Current	V_{FBL} = 0.5V	250			mA
LOUT Load Regulation	V_{LIN} = 5V, 5mA < I_{OUT} < 250mA, not in dropout			1	%
Soft-Start Period	7-bit voltage ramp		3		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{LIN} = V_{EN} = +3.3V, circuit of Figure 2, V_{MAIN} = 8V, V_{GON1} = V_{GON2} = 21V, V_{GOFF} = -6.5V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
STEP-UP DC-DC CONVERTER					
Switching Frequency	f (MHz) = 0.015 x R_{FREQ} (kΩ), R_{FREQ} = 80kΩ	1000	1200	1500	kHz
	f (MHz) = 0.015 x R_{FREQ} (kΩ), R_{FREQ} = 30kΩ	382	450	518	
	f (MHz) = 0.015 x R_{FREQ} (kΩ), R_{FREQ} = unconnected	570	600	690	
Oscillator Maximum Duty Cycle		88	92	96	%
FB Regulation Voltage		1.216	1.235	1.254	V
FB Load Regulation	0 < I_{MAIN} < 200mA, transient only		-1		%
FB Line Regulation	V_{IN} = 1.8V to 5.5V	-0.15	-0.08	+0.15	%/V
FB Input Bias Current	V_{FB} = 1.3V	25	75	150	nA
FB Transconductance	ΔI = 5µA at COMP	75	160	280	µS
FB Voltage Gain	FB to COMP		2400		V/V
LX On-Resistance	I_{LX} = 200mA		150	250	mΩ
LX Leakage Current	V_{LX} = 16V		10	20	µA
LX Current Limit	Duty cycle = 65%	2	2.5	3	A
Current-Sense Transresistance		0.15	0.3	0.45	V/A
Soft-Start Period	C_{SS} < 200pF		10		ms
SS Output Current		3.5	5	6.5	µA
HIGH-VOLTAGE DRIVER BLOCK					
GON1, GON2 Input Voltage		12		30	V
GOFF Input Voltage		-10		-4	V
GOFF Supply Current	A2–A8 = AGND, no load		120	250	µA
GON1, GON2 Supply Current	A2–A8 = AGND, no load		265	430	µA
Output-Voltage Low (Y2–Y8, YDCHG)	I_{OUT} = 10mA		V_{GOFF} + 0.3	V_{GOFF} + 1	V
Output-Voltage High (Y2–Y8, YDCHG)	I_{OUT} = 10mA	$V_{GON\_}$ - 1	$V_{GON\_}$ - 0.3		V
Rise Time (Y2–Y8)	C_{LOAD} = 100pF, V_{GON1} = V_{GON2} = 30V, V_{GOFF} = -10V (Note 1)		16	32	ns
Fall Time (Y2–Y8)	C_{LOAD} = 100pF, V_{GON1} = V_{GON2} = 30V, V_{GOFF} = -10V (Note 1)		16	32	ns
Propagation Delay High-to-Low Transition (Y2–Y8)	C_{LOAD} = 100pF (Note 1)		80	125	ns
Propagation Delay Low-to-High Transition (Y2–Y8)	C_{LOAD} = 100pF (Note 1)		80	125	ns
Operating Frequency	C_{LOAD} = 100pF			50	kHz

Internal-Switch Boost Regulator with Integrated 7-Channel Driver, VCOM Calibrator, Op Amp, and LDO

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{LIN} = V_{EN} = +3.3V, circuit of Figure 2, V_{MAIN} = 8V, V_{GON1} = V_{GON2} = 21V, V_{GOFF} = -6.5V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OPERATIONAL AMPLIFIER					
AVDD Supply Voltage Range		6		14	V
AVDD Overvoltage Threshold	Rising edge, 400mV hysteresis	14.1	15	15.9	V
AVDD Input Supply Current	FB = 1.1V, buffer configuration, V_{POS} = V_{AVDD}/2, no load		5	10	mA
Input Offset Voltage	V_{NEG}, V_{POS} = V_{AVDD}/2, T_A = +25°C	-12		+12	mV
Input Bias Current	V_{NEG}, V_{POS} = V_{AVDD}/2, T_A = +25°C	-50		+50	nA
Input Common-Mode Voltage Range		0		V_{AVDD}	V
Input Common-Mode Rejection Ratio			80		dB
Output-Voltage Swing High	I_{OUT} = 50mA	V_{AVDD} - 300			mV
Output-Voltage Swing Low	I_{OUT} = -50mA			300	mV
Large-Signal Voltage Gain	V_{OUT} = 1V to V_{AVDD} - 1V		80		dB
Slew Rate			45		V/µs
-3dB Bandwidth			20		MHz
Short-Circuit Current	Short to V_{AVDD} - 3V sourcing	200			mA
	Short to 3V sinking	200			
CONTROL INPUTS					
Logic-Input Voltage Low (A2–A8, EN)	1.8V < V_{IN} < 5.5V			0.8	V
Logic-Input Voltage High (A2–A8, EN)	1.8V < V_{IN} < 5.5V	1.6			V
Logic-Input Bias Current (A2–A8)	0 < A_X < V_{IN}, T_A = +25°C	-1		+1	µA
Logic-Input Bias Current (EN)	0 < V_{EN} < V_{IN}, T_A = +25°C	-1		+1	µA
INPUT-VOLTAGE DETECTOR					
SENSE Voltage Range				V_{VL}	V
SENSE Bias Current	0 < V_{SENSE} < V_L, T_A = +25°C	-1		+1	µA
SENSE Threshold Voltage	Falling edge	1.200	1.235	1.270	V
PROGRAMMABLE VCOM CALIBRATOR					
GON2 Calibrating Threshold	Rising edge, 230mV hysteresis	7	8.5	10.5	V
GON2 Input-Voltage Range		11		30	V
SET Voltage Resolution		7			Bits
SET Differential Nonlinearity		-1		+1	LSB
SET Zero-Scale Error		-1	+1	+3	LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{LIN} = V_{EN} = +3.3V, circuit of Figure 2, V_{MAIN} = 8V, V_{GON1} = V_{GON2} = 21V, V_{GOFF} = -6.5V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SET Full-Scale Error		-4		+5	LSB
SET Current				120	µA
SET External Resistance	To GND, V_{AVDD} = 14V	8.5		170	kΩ
	To GND, V_{AVDD} = 6V	2.5		50	
V_{SET}/V_{AVDD} Voltage Ratio	DAC zero scale		0.05		V/V
POS Settling Time	To ±0.5 LSB error band		20		µs
Memory Write Cycles		30			Times
Memory Write Time	R_{FREQ} = unconnected	150			ms
I²C INTERFACE					
Logic-Input Low Voltage (V_{IL})	SDA, SCL			0.3 x V_{IN}	V
Logic-Input Low Voltage	ADDR0_ADDR1			0.2 x V_{IN}	V
Logic-Input High Voltage (V_{IH})	SDA, SCL, ADDR0, ADDR1	0.7 x V_{IN}			V
SDA Output Low Voltage	I_{SDA} = -3mA sink	0		0.4	V
Logic-Input Current	SDA, SCL, ADDR0, ADDR1, T_A = +25°C	-1		+1	µA
SDA and SCL Input Capacitance	(Note 1)		5	10	pF
SCL Frequency (f_{SCL})		DC		400	kHz
SCL High Time (t_{HIGH})		600			ns
SCL Low Time (t_{LOW})		1300			ns
SDA and SCL Rise Time and Fall (t_R, t_F)	Cb = total capacitance of bus line in pF (Note 1)	20 + 0.1 x Cb		300	ns
START Condition Hold Time ($t_{HD:STA}$)	10% of SDA to 90% of SCL	600			ns
START Condition Setup Time ($t_{SU:STA}$)		600			ns
Data Input Hold Time ($t_{HD:DAT}$)		50			ns
Data Input Setup Time ($t_{SU:DAT}$)		100			ns
STOP Condition Setup Time ($t_{SU:STO}$)		600			ns
Bus Free Time (t_{BUF})		1300			ns
SDA Capacitive Loading (Cb)	(Note 2)			400	pF
Input Filter Spike Suppression	SDA, SCL, not tested			50	ns

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{LIN} = V_{EN} = +3.3V, circuit of Figure 2, V_{MAIN} = 8V, V_{GON1} = V_{GON2} = 21V, V_{GOFF} = -6.5V. **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL						
IN Input-Voltage Range			1.8		5.5	V
IN Shutdown Current	EN = 0, V_L > 2.4V				100	µA
IN Quiescent	V_{IN} = 3V, V_{FB} = 1.5V, not switching				100	µA
IN Undervoltage Lockout	V_{IN} rising				1.75	V
BOOTSTRAP LINEAR REGULATOR (VL)						
VL Output Voltage			3.8		4.2	V
VL Maximum Output Current	VL = 3.7V		10			mA
LINEAR REGULATOR						
LIN Input-Voltage Range	V_{LOUT} < V_{LIN}		1.8		5.5	V
LIN Quiescent Current	No load				2	mA
Dropout Voltage	I_{LOUT} = 250mA				0.3	V
FBL Regulation Voltage	I_{LOUT} = 100mA		605		631	mV
LOUT Maximum Output Current	V_{FBL} = 0.5V		250			mA
LOUT Load Regulation	V_{LIN} = 5V, 5mA < I_{OUT} < 250mA, not in dropout				1	%
STEP-UP DC-DC CONVERTER						
Output-Voltage Range			6		14	V
Switching Frequency	f (MHz) = 0.015 x R_{FREQ} (kΩ)	R_{FREQ} = 80kΩ	1000		1500	kHz
		R_{FREQ} = 30kΩ	382		518	
		R_{FREQ} = unconnected	510		690	
Oscillator Maximum Duty Cycle			88		96	%
FB Regulation Voltage			1.216		1.254	V
LX On-Resistance	I_{LX} = 200mA				250	mΩ
LX Leakage Current	V_{LX} = 16V				20	µA
LX Current Limit	Duty cycle = 65%		2		3	A
Current-Sense Transresistance			0.15		0.45	V/A
SS Output Current			3.5		6.5	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{LIN} = V_{EN} = +3.3V, circuit of Figure 2, V_{MAIN} = 8V, V_{GON1} = V_{GON2} = 21V, V_{GOFF} = -6.5V. **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-VOLTAGE DRIVER BLOCK					
GON1, GON2 Input Voltage		12		30	V
GOFF Input Voltage		-10		-4	V
GOFF Supply Current	A2–A8 = AGND, no load			250	µA
GON1, GON2 Supply Current	A2–A8 = AGND, no load			430	µA
Output-Voltage Low (Y2–Y8)	I_{OUT} = 10mA			V_{GOFF} + 1	V
Output-Voltage High (Y2–Y8)	I_{OUT} = 10mA	$V_{GON\_}$ - 1			V
Rise Time (Y2–Y8)	C_{LOAD} = 100pF, V_{GON1} = V_{GON2} = 30V, V_{GOFF} = -10V (Note 1)			32	ns
Fall Time (Y2–Y8)	C_{LOAD} = 100pF, V_{GON1} = V_{GON2} = 30V, V_{GOFF} = -10V (Note 1)			32	ns
Propagation Delay High-to-Low Transition (Y2–Y8)	C_{LOAD} = 100pF (Note 1)			125	ns
Propagation Delay Low-to-High Transition (Y2–Y8)	C_{LOAD} = 100pF (Note 1)			125	ns
Operating Frequency	C_{LOAD} = 100pF			50	kHz
OPERATIONAL AMPLIFIER					
AVDD Supply Voltage Range		6		14	V
AVDD Overvoltage Threshold	Rising edge, 400mV hysteresis	14.1		15.9	V
AVDD Input Supply Current	FB = 1.1V, buffer configuration, V_{POS} = V_{AVDD}/2, no load			10	mA
Input Common-Mode Voltage Range		0		V_{AVDD}	V
Output-Voltage Swing High	I_{OUT} = 50mA	V_{AVDD} - 300			mV
Output-Voltage Swing Low	I_{OUT} = -50mA			300	mV
Short-Circuit Current	Short to V_{AVDD} - 3V sourcing	200			mA
	Short to 3V sinking	200			
CONTROL INPUTS					
Logic-Input Voltage Low (A2–A8, EN)	1.8V < V_{IN} < 5.5V			0.8	V
Logic-Input Voltage High (A2–A8, EN)	1.8V < V_{IN} < 5.5V	1.6			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{LIN} = V_{EN} = +3.3V, circuit of Figure 2, V_{MAIN} = 8V, V_{GON1} = V_{GON2} = 21V, V_{GOFF} = -6.5V. **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT-VOLTAGE DETECTOR					
SENSE Voltage Range				V_{VL}	V
SENSE Threshold Voltage	Falling edge, 10mV (typ) hysteresis	1.200		1.270	V
PROGRAMMABLE VCOM CALIBRATOR					
GON2 Calibrator Threshold	Rising edge, 230mV hysteresis	7	8.5	10.5	V
GON1 Voltage Threshold to Enable Program	Rising edge, 230mV hysteresis	7		10.5	V
GON2 Input-Voltage Range		11		30	V
SET Voltage Resolution		7			Bits
SET Differential Nonlinearity		-1		+1	LSB
SET Zero-Scale Error		-1	+1	+3	LSB
SET Full-Scale Error		-4		+5	LSB
SET Current				120	µA
SET External Resistance	To GND, V_{AVDD} = 14V	8.5		170	kΩ
	To GND, V_{AVDD} = 6V	2.5		50	kΩ
Memory Write Cycles		30			Times
Memory Write Time	R_{FREQ} = unconnected	150			ms
I²C INTERFACE					
Logic-Input Low Voltage (V_{IL})	SDA, SCL			0.3 x V_{IN}	V
Logic-Input Low Voltage	ADDR0, ADDR1			0.2 x V_{IN}	V
Logic-Input High Voltage (V_{IH})	SDA, SCL, ADDR0, ADDR1	0.7 x V_{IN}			V
SDA Output Low Voltage	I_{SDA} = -3mA sink	0		0.4	V
SDA and SCL Input Capacitance	SDA, SCL (Note 1)			10	pF
SCL Frequency (f_{SCL})		DC		400	kHz
SCL High Time (t_{HIGH})		600			ns
SCL Low Time (t_{LOW})		1300			ns
SDA and SCL Rise and Fall Time (t_R, t_F)	Cb = total capacitance of bus line in pF (Note 1)	20 + 0.1 x Cb		300	ns
START Condition Hold Time ($t_{HD:STA}$)	10% of SDA to 90% of SCL	600			ns
START Condition Setup Time ($t_{SU:STA}$)		600			ns
Data Input Hold Time ($t_{HD:DAT}$)		50			ns
Data Input Setup Time ($t_{SU:DAT}$)		100			ns
STOP Condition Setup Time ($t_{SU:STO}$)		600			ns
Bus Free Time (t_{BUF})		1300			ns
SDA Capacitive Loading (Cb)	(Note 2)			400	pF
Input Filter Spike Suppression	SDA, SCL, not tested			50	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{LIN} = V_{EN} = +3.3V, circuit of Figure 2, V_{MAIN} = 8V, V_{GON1} = V_{GON2} = 21V, V_{GOFF} = -6.5V. **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

Note 1: Guaranteed by design, not production tested.
Note 2: The maximum amount capacitance allowed on the SDA bus lines.
Note 3: T_A = -40°C specifications are guaranteed by design, not production tested.

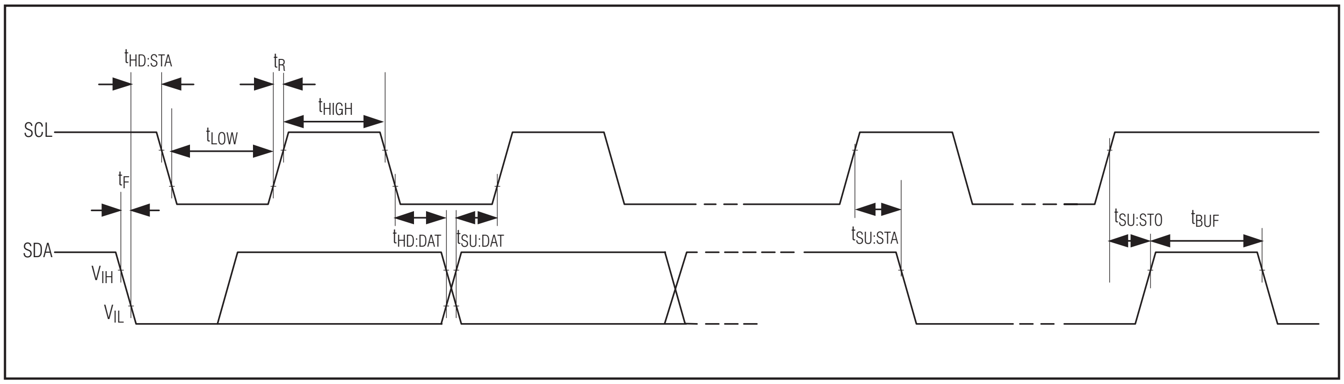
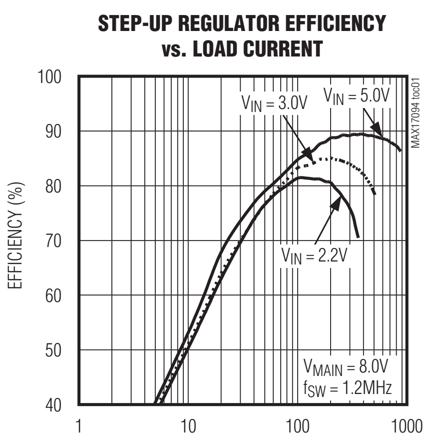
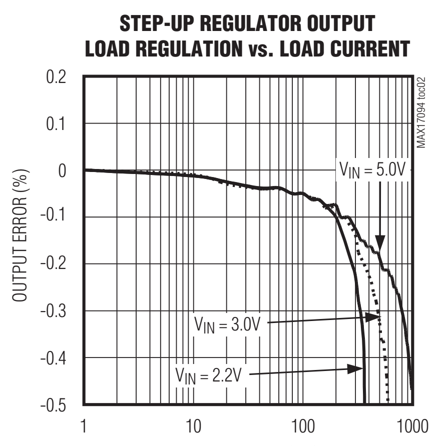


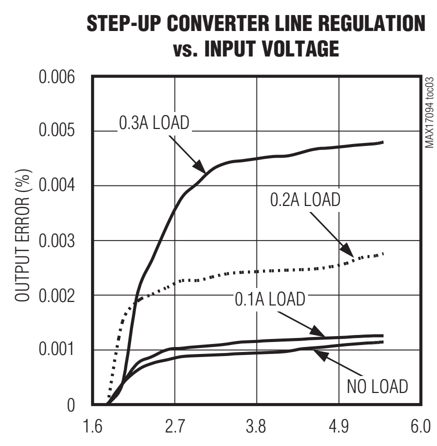
Figure 1. Timing Definitions Used in the Electrical Characteristics

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)



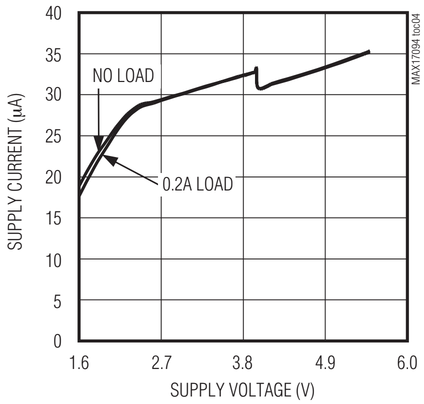




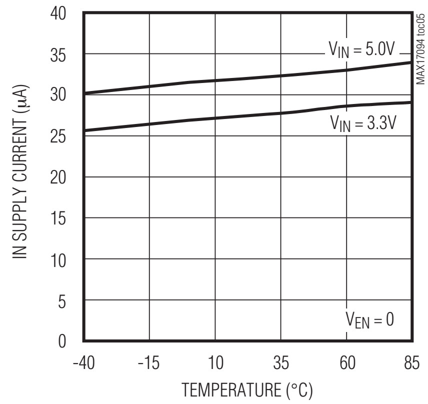
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

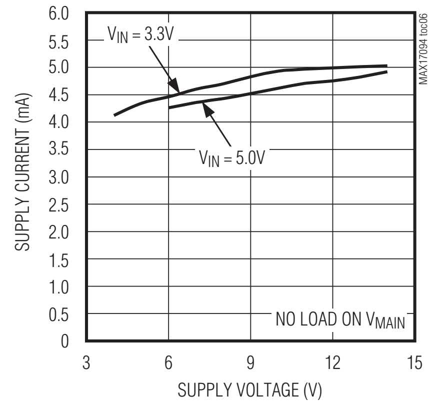
IN SUPPLY QUIESCENT CURRENT vs. IN SUPPLY VOLTAGE



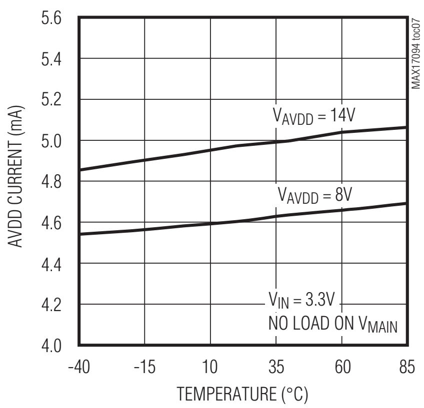
IN SUPPLY QUIESCENT CURRENT vs. TEMPERATURE



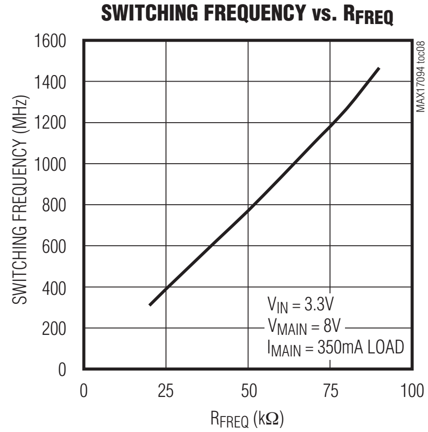
AVDD SUPPLY CURRENT vs. AVDD SUPPLY VOLTAGE



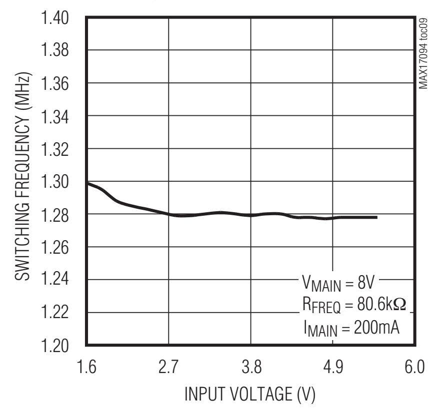
AVDD CURRENT vs. TEMPERATURE



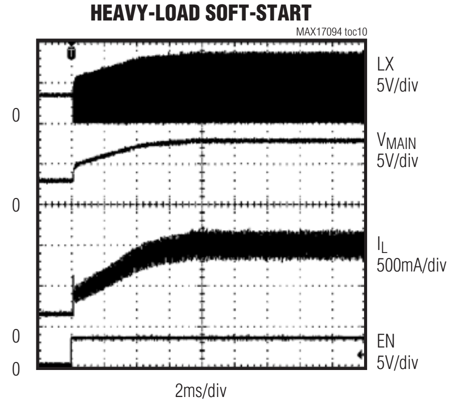
STEP-UP CONVERTER SWITCHING FREQUENCY vs. R_{FREQ}



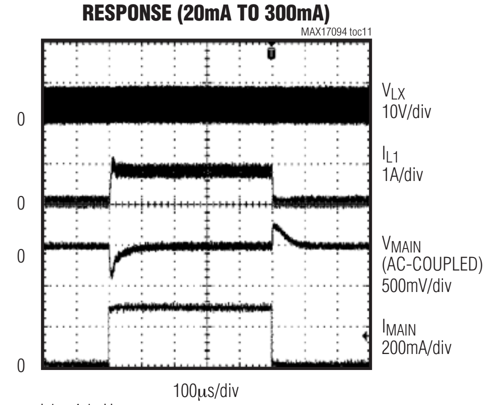
STEP-UP CONVERTER SWITCHING FREQUENCY vs. INPUT VOLTAGE



STEP-UP REGULATOR HEAVY-LOAD SOFT-START



STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE (20mA TO 300mA)

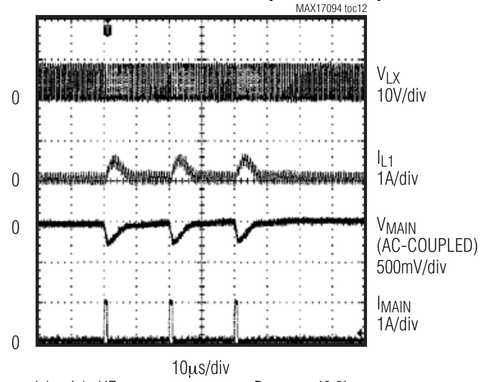


L1 = 4.1µH
R_{COMP} = 40.2kΩ
C_{COMP} = 1000pF

Typical Operating Characteristics (continued)

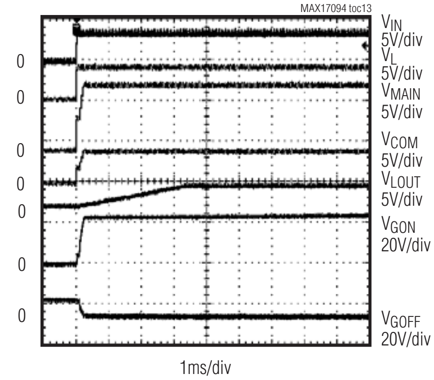
(T_A = +25°C, unless otherwise noted.)

STEP-UP REGULATOR PULSED LOAD-TRANSIENT RESPONSE (20mA TO 1A)

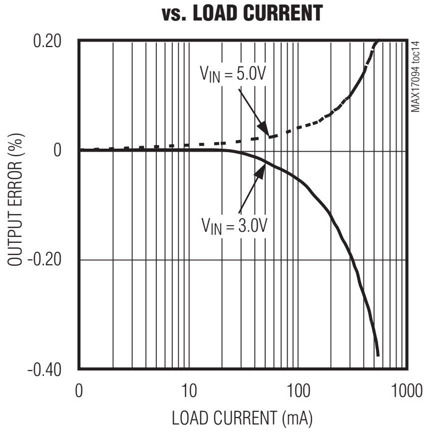


L1 = 4.1µHF RCOMP = 40.2kΩ CCOMP = 1000pF

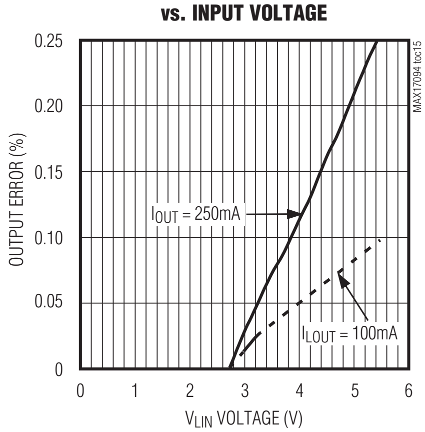
POWER-UP SEQUENCE OF ALL SUPPLY OUTPUTS



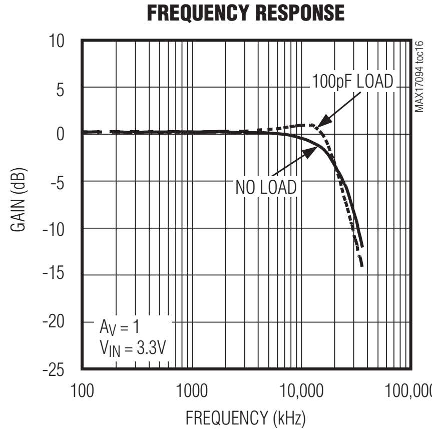
LDO OUTPUT REGULATION vs. LOAD CURRENT



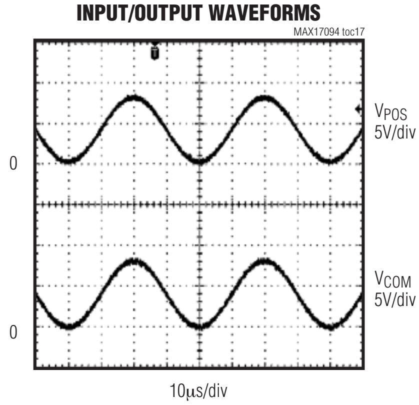
LDO OUTPUT LINE REGULATION vs. INPUT VOLTAGE



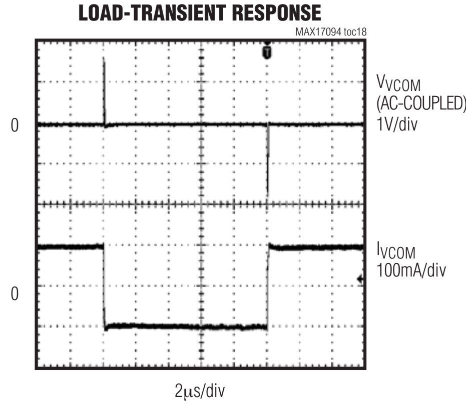
OPERATIONAL AMPLIFIER FREQUENCY RESPONSE



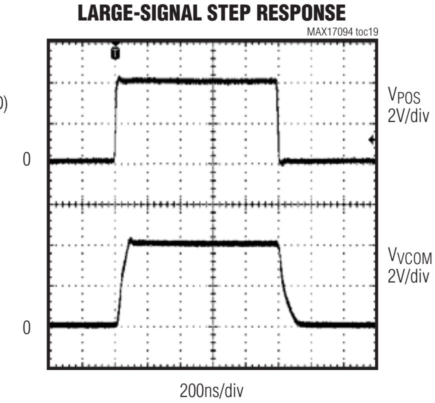
OPERATIONAL AMPLIFIER RAIL-TO-RAIL INPUT/OUTPUT WAVEFORMS



OPERATIONAL AMPLIFIER LOAD-TRANSIENT RESPONSE



OPERATIONAL AMPLIFIER LARGE-SIGNAL STEP RESPONSE

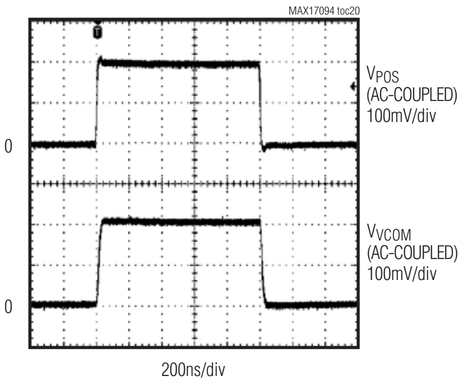


Internal-Switch Boost Regulator with Integrated 7-Channel Driver, VCOM Calibrator, Op Amp, and LDO

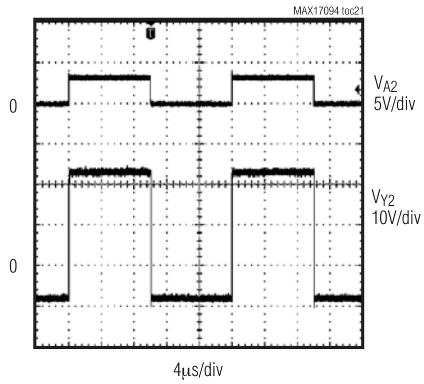
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

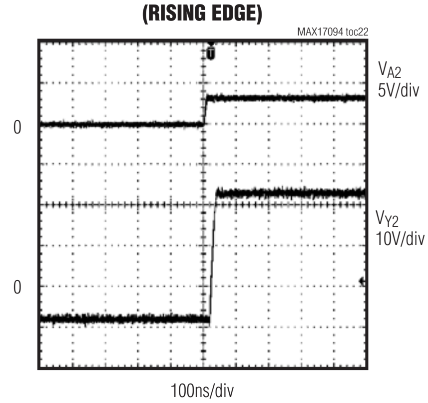
OPERATIONAL AMPLIFIER SMALL-SIGNAL STEP RESPONSE



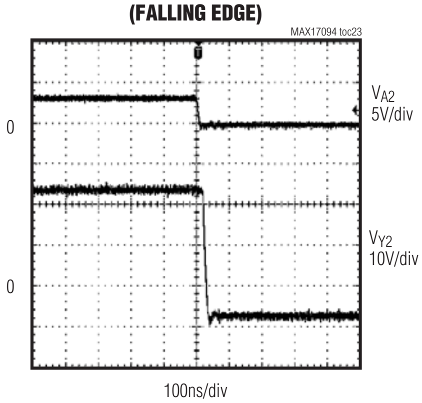
SCAN DRIVER INPUT/OUTPUT WAVEFORMS WITH LOGIC INPUT



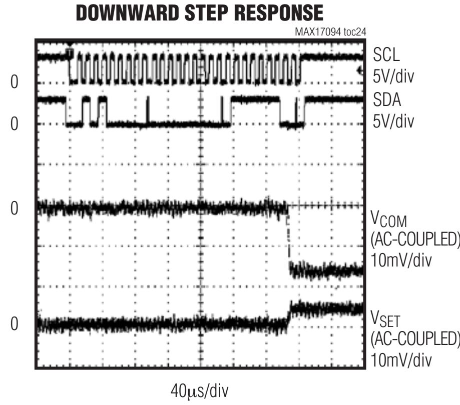
SCAN DRIVER PROPAGATION DELAY (RISING EDGE)



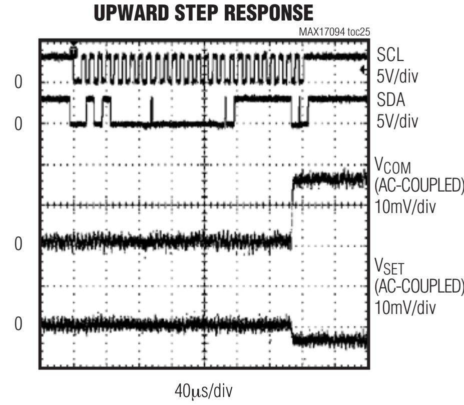
SCAN DRIVER PROPAGATION DELAY (FALLING EDGE)



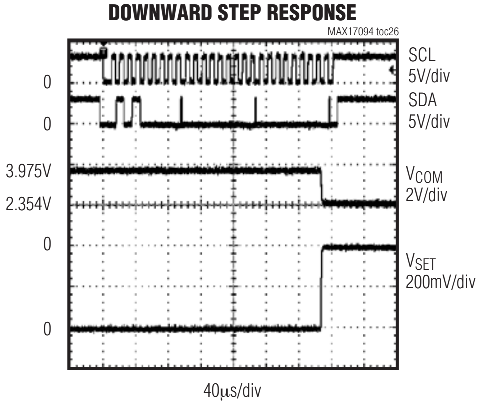
CALIBRATION SIGNAL LSB DOWNWARD STEP RESPONSE



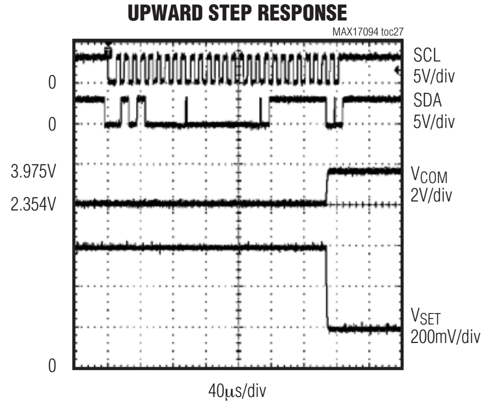
CALIBRATION SIGNAL LSB UPWARD STEP RESPONSE



CALIBRATION FULL-SCALE DOWNWARD STEP RESPONSE



CALIBRATION FULL-SCALE UPWARD STEP RESPONSE



Pin Description

PIN	NAME	FUNCTION
1	LIN	Input of the Internal Linear Regulator. Bypass LIN to GND with a 4µF capacitor close to the IC.
2	LOUT	Internal Linear Regulator Output. Bypass LOUT to GND with a 4.7µF capacitor.
3	FBL	Linear Regulator Feedback Pin. Connect external resistor-divider tap here and minimize trace area. Set V_{LOGIC} according to: V_{LOGIC} = 0.618V x (1 + R7/R8) (Figure 2).
4, 26, 29	GND	Analog Ground
5	ADDR0	Address Select Pin to Set Address for the I^2C Slave Address
6	ADDR1	Address Select Pin to Set Address for the I^2C Slave Address
7	SCL	I^2C-Compatible Clock Input
8	SDA	I^2C-Compatible Serial Bidirectional Data Line
9–15	A2–A8	Level-Shifter Logic-Level Inputs
16	SS	Step-Up Regulator Soft-Start Control. Connect a capacitor greater than 200pF between SS and AGND to set the step-up regulator soft-start timing. SS is connected to AGND when EN is low. When EN goes high, the capacitor at SS is charged by an internal 5µA current source, slowly raising the internal current limit. The full LX current limit is available when V_{SS} = 1.235V or when V_{MAIN} reaches its regulation threshold, whichever occurs first. If no capacitor is connected, the soft-start time is controlled by an internal 10ms digital timer.
17	YDCHG	Level-Shifter Output Used to Discharge the Panel
18–24	Y2–Y8	Level-Shifter Outputs
25	GOFF	Gate-Off Supply. GOFF is the negative supply voltage for the Y2–Y8 and YDCHG level-shifter circuitry. Bypass to GND with a minimum 0.1µF ceramic capacitor.
27	GON2	Gate-On Supply. GON2 is the positive supply for the Y7 and Y8 level-shifter circuitry. Bypass to GND with a minimum 0.1µF ceramic capacitor.
28	GON1	Gate-On Supply. GON1 is the positive supply for the Y2–Y6 and YDCHG level-shifter circuitry. Bypass to GND with a minimum 0.1µF ceramic capacitor.
30	SET	Full-Scale, Sink-Current Adjustment Input. Connect a resistor, R_{SET}, from SET to GND to set the full-scale adjustable sink current, which is V_{AVDD}/(20 x R_{SET}). I_{OUT} is equal to the current through R_{SET}.
31	BGND	Operational Amplifier GND
32	VCOM	Operational Amplifier Output
33	NEG	Operational Amplifier Negative Input
34	POS	Operational Amplifier Positive Input
35	OUT	Adjustable Sink-Current Output. OUT connects to the resistive voltage-divider at the op amp input POS (between AVDD and BGND) that determines the VCOM output voltage. I_{OUT} lowers the divider voltage by a programmable amount.
36	AVDD	Op Amp and Internal VL Linear Regulator Supply Input. Bypass AVDD to BGND with a 0.1µF capacitor.
37	FB	Step-Up Regulator Feedback. Connect external resistor-divider tap here and minimize trace area. Set V_{OUT} according to: V_{OUT} = 1.235V x (1 + R1/R2) (Figure 2).
38, 39	PGND	Power Ground
40, 41	LX	Switching Node. Connect inductor/catch diode here and minimize trace area for lowest EMI.
42	FREQ	SMPS Frequency Adjust. Connect a resistor between 30kΩ and 80kΩ to select the step-up converter's operating frequency as determined by: f (mHz) = 0.015 x R_{FREQ} (kΩ). Leave unconnected for f = 600kHz.

Internal-Switch Boost Regulator with Integrated 7-Channel Driver, VCOM Calibrator, Op Amp, and LDO

Pin Description (continued)

PIN	NAME	FUNCTION
43	EN	Enable. Pull EN low to turn off the DC-DC converter and the op amp. The high-voltage scan drivers and LDO remain active if sufficient voltage is available for operation.
44	IN	Supply. Bypass to AGND with a minimum 0.1µF ceramic capacitor.
45	SENSE	Input-Voltage Threshold Detector. Connect this pin to V_{IN} through a resistor-divider. When the voltage at the SENSE pin falls below a 1.235V threshold, YDCHG is driven to V_{GON1}.
46	COMP	Compensation Pin for Error Amplifier. Connect a series RC from COMP to AGND. Typical values are 40.2kΩ and 1000pF.
47	AGND	Analog GND
48	VL	On-Chip Regulator Output. This regulator powers internal analog circuitry. Bypass VL to AGND with a 0.22µF or greater ceramic capacitor.
—	EP	Exposed Backside Pad. Connect to AGND and make AGND copper plane as level as possible to help external dissipation.

Table 1. Component List

DESIGNATION	DESCRIPTION
C1	4.7µF ±10%, 6.3V X5R ceramic capacitor (0603) Murata GRM188R60J475K TDK C1608X5R0J475K
C2, C3	1µF ±20%, 6.3V X5R ceramic capacitors (0402) Murata GRM155R60J105K TDK C1005X5R0J105M
C4	10µF ±20%, 6.3V X5R ceramic capacitor (0603) Murata GRM188R60J106M TDK C1608X5R0J106K
C5, C6	4.7µF ±10%, 16V X5R ceramic capacitors (0805) Murata GRM21BR61C475K Taiyo Yuden EMK212BJ475KG
D1	30V Schottky diode, 1A (S-Flat) Toshiba CRS02
L1	4.1µH, 1.95A, 57mΩ inductor (6mm x 6mm x 2mm) Sumida CDRH5D18NP-4R1NC Coiltronics SD6020-4R1-R

Typical Operating Circuit

The MAX17094 typical operating circuit (Figure 2) generates a +8V source-driver supply and approximately +22V and -6.5V gate-driver supplies for TFT displays. The input-voltage range for the IC is from +1.8V to +5.5V, but the Figure 2 circuit is designed to run from 2.5V to 3.6V. Table 1 lists the recommended components and Table 2 lists the component suppliers. Figure 3 is the MAX17094 functional diagram.

Table 2. Component Suppliers

SUPPLIER	WEBSITE
Coiltronics	www.cooperet.com
Murata Electronics North America, Inc.	www.murata-northamerica.com
Sumida Corp.	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
Toshiba America Electronic Components, Inc.	www.toshiba.com/taec

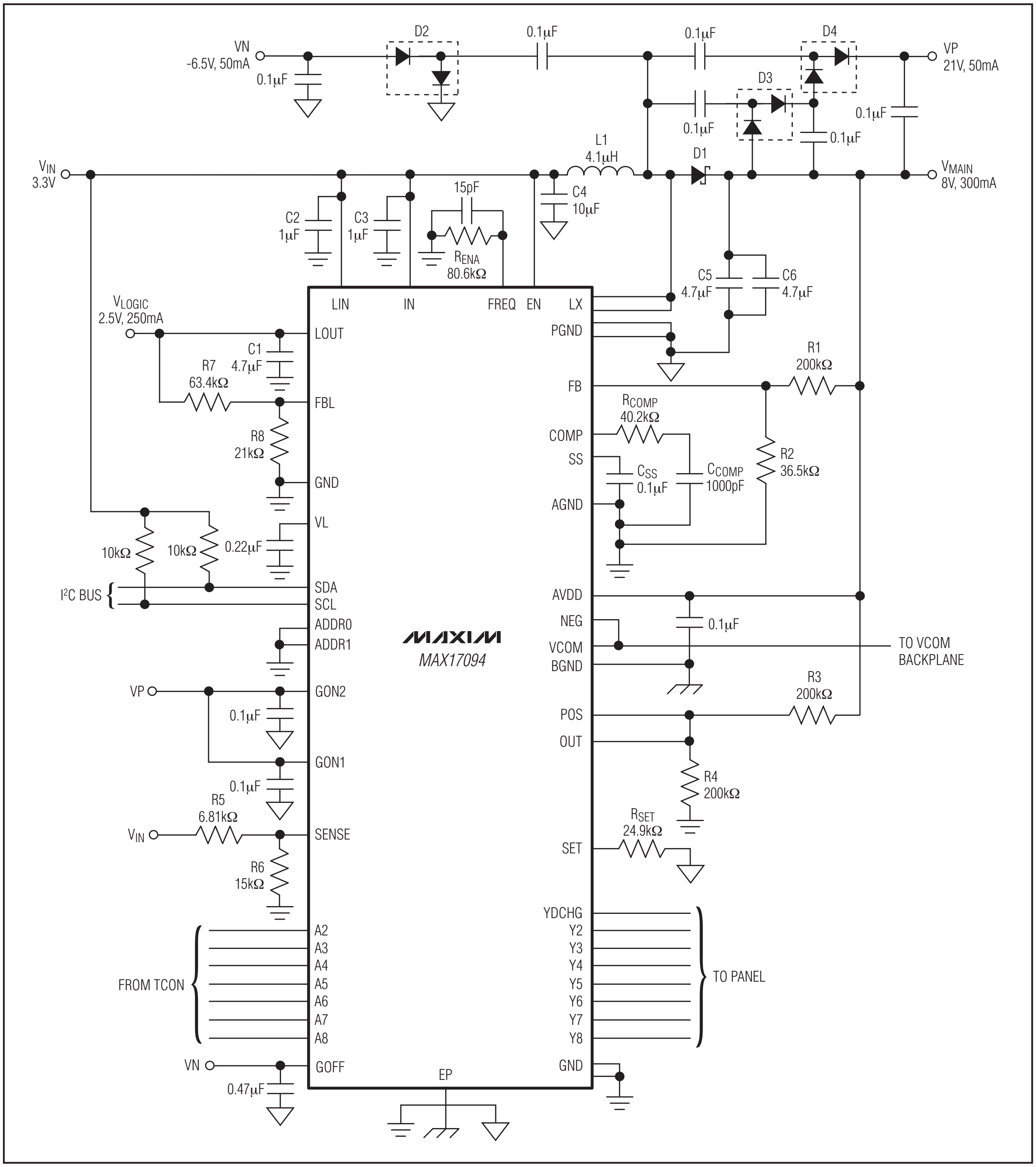


Figure 2. MAX17094 Typical Operating Circuit

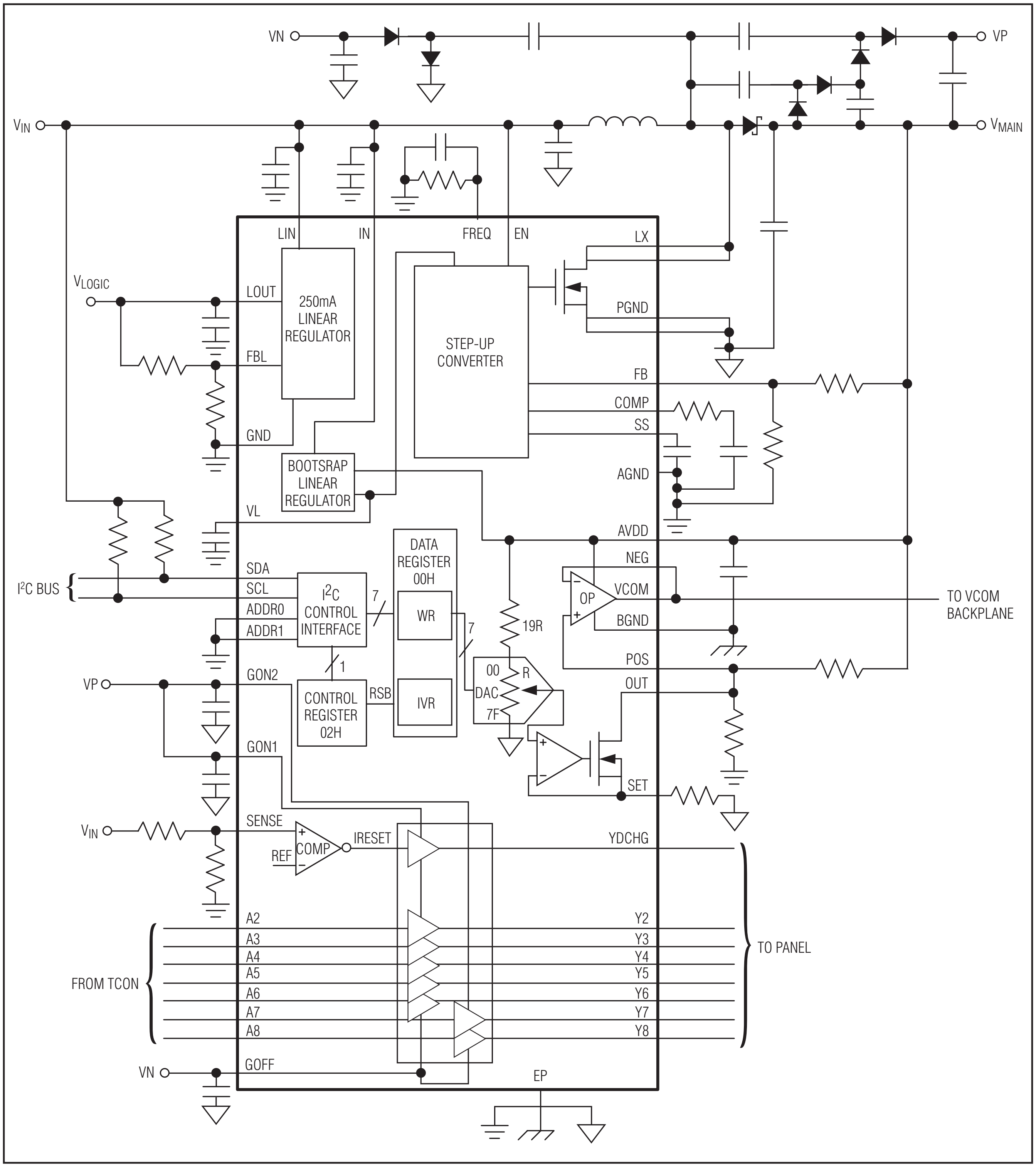


Figure 3. MAX17094 Functional Diagram

Detailed Description

The MAX17094 includes a high-performance step-up regulator, a 250mA LDO linear regulator, a high-speed operational amplifier, a digitally adjustable VCOM calibration device with nonvolatile memory and I^2C interface, and a high-voltage, level-shifting scan driver optimized for active-matrix TFT LCDs.

Step-Up Regulator

The step-up regulator employs a peak current-mode control architecture with an adjustable (600kHz to 1.2MHz), constant-switching frequency that maximizes loop bandwidth and provides a fast-transient response to pulsed loads found in source drivers of TFT LCD panels. The high switching frequency is programmable from 450kHz to 1.2MHz by selecting an appropriate external resistor connected between the FREQ input and AGND. The high switching frequency also allows the use of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. The integrated high-efficiency MOSFET and the IC's built-in digital soft-start functions reduce the number of external components required while controlling inrush current. The output voltage can be set from V_{IN} to 14V with an external resistive voltage-divider.

The regulator controls the output voltage and the power delivered to the output by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{MAIN} - V_{IN}}{V_{MAIN}}$$

Figure 4 shows the block diagram of the step-up regulator. An error amplifier compares the signal at FB to 1.235V and changes the COMP output. The voltage at COMP determines the current trip point each time the internal MOSFET turns on. As the load varies, the error amplifier sources or sinks current to the COMP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope compensation signal is summed with the current-sense signal.

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceed the COMP voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the diode (D1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit compares the input voltage at IN with the UVLO (1.3V typ) to ensure that the input voltage is high enough for reliable operation. The 200mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO-rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the main step-up regulator and the linear regulator, disables the switch-control block, and the operational amplifier output becomes high impedance.

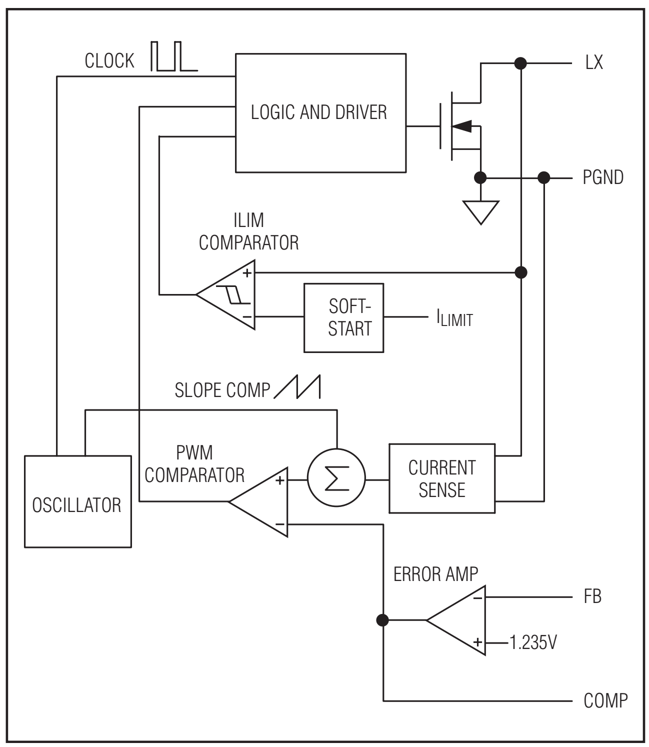


Figure 4. Step-Up Regulator Block Diagram

Internal-Switch Boost Regulator with Integrated 7-Channel Driver, VCOM Calibrator, Op Amp, and LDO

Soft-Start

The soft-start feature effectively limits the inrush current during startup by linearly ramping up the step-up converter's peak switch current limit. The soft-start period terminates when either the output voltage reaches regulation or the full current limit has been reached. By default, the current limit is controlled by an internal timer that allows the current limit to rise from 0 to the full current limit in approximately 10ms. If an adjustable soft-start period is desired, an external capacitor (C_{SS}) greater than 200pF can be connected between SS and GND. In this case, C_{SS} is charged with a 5µA current source such that the full current limit is reached until the voltage across C_{SS} reaches 1.235V.

Fault Protection

The MAX17094 monitors AVDD for an overvoltage condition. If the AVDD voltage is above 14.1V (min), the MAX17094 disables the gate driver of the step-up regulator and prevents the internal MOSFET from switching. The AVDD overvoltage condition does not set the fault latch.

Operational Amplifier

The MAX17094 has an operational amplifier that is typically used to drive the LCD backplane (VCOM). The operational amplifier features ±200mA output short-circuit current, 45V/µs slew rate, and 20MHz bandwidth. While the op amp is a rail-to-rail input and output design, its accuracy is significantly degraded for input voltages within 1V of its supply rails (AVDD and BGND).

Short-Circuit Current Limit

The operational amplifier limits short-circuit current to approximately ±200mA if the output is directly shorted to AVDD or to AGND. If the short-circuit condition persists, the junction temperature of the IC rises until it reaches the thermal-shutdown threshold (+160°C typ). Once the junction temperature reaches the thermal-shutdown threshold, an internal thermal sensor immediately sets the thermal-fault latch, shutting off the main step-up regulator, the linear regulator, the switch-control block, and the operational amplifier. Those portions of the device remain inactive until the input voltage is cycled off, then on, again.

Driving Pure Capacitive Loads

The operational amplifier is typically used to drive the LCD backplane (VCOM) or the gamma-correction-divider string. The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by the operational amplifier. However, if the operational amplifier is used in an application with a pure capacitive load, steps must be taken to ensure stable operation. As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A 5Ω to 50Ω small resistor placed between VCOM and the capacitive load reduces peaking, but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between 100Ω and 200Ω and the typical value of the capacitor is 10pF.

High-Voltage Level-Shifting Scan Driver

The MAX17094 includes seven logic-level to high-voltage level-shifting buffers, which can buffer seven logic inputs (A2–A8) and shift them to a desired level (Y2–Y8) to drive TFT-LCD row logic. The driver outputs, Y2–Y8, swing between their power-supply rails, according to the input-logic level on A2–A8. The driver output is GOFF when its respective input is logic low, and GON_ when its respective input is logic high. These seven driver channels are grouped for different high-level supplies. A2–A6 are supplied from GON1, and A7 and A8 are supplied from GON2. GON1 and GON2 can be tied together to make A2–A8 use identical supplies. The high-voltage, level-shifting scan drivers are designed to drive the TFT panels with row drivers integrated on the panel glass. Its seven outputs swing from +30V (max) to -10V (min) and can swiftly drive capacitive loads. The typical propagation delays are 80ns, with fast 16ns rise-and-fall times. The buffers can operate at frequencies up to 50kHz. A YDCHG is the output of the eight-level shifting buffer. It is driven by the input-voltage-detector circuit.

Input-Voltage Detector

The input-voltage detector is used to drive the YDCHG level-shifter buffer to V_{GON1} during a power-down once the input voltage has fallen below a user-defined threshold. The input voltage is sensed at the SENSE pin through a voltage-divider. Once the falling edge of V_{SENSE} falls below 1.235V (typ), YDCHG is driven to V_{GON1}.

Low-Dropout Linear Regulator (LDO)

The MAX17094 has an integrated 1.2Ω (max) pass element and can provide at least 250mA. The output voltage is accurate within ±2%.

VCOM Calibrator

The VCOM calibrator is a solid-state alternative to mechanical potentiometers used for adjusting the LCD backplane voltage (VCOM) in TFT LCD displays. OUT attaches to the external resistive voltage-divider at the POS terminal of the op amp and sinks a programmable current (I_{OUT}), which sets the VCOM levels (Figure 5). The DAC setting that controls the wiper setting of the potentiometer is directly determined by the value stored in the wiper register (WR). Changing the value in WR allows the user to change the wiper position to increase or decrease the VCOM levels. The user can store a WR setting into the nonvolatile initial value register (IVR) such that on power-up, WR is preset to the last stored value in IVR. The 2-wire I^2C interface between the system controller and the programming circuit adjusts WR and programs IVR. The resistive voltage-divider and AVDD supply set the maximum value of VCOM. OUT sinks current from the voltage-divider to reduce the POS voltage level and VCOM output. The external resistor at SET (R_{SET}) sets the full-scale sink current and the minimum value of VCOM.

The GON2 input provides the high voltage required to program IVR. GON2 is connected to the TFT LCD V_{GON2} supply. V_{GON2} should be between 12V and 30V. IVR programming is guaranteed only when GON2 is greater than 7V. Bypass GON2 to GND (which is bypassed to GND) with a 0.1µF or greater capacitor.

Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the device. When the junction temperature exceeds T_J = +160°C, a thermal sensor immediately activates the fault protection, which shuts down the step-up regulator, LDO, and the operational amplifiers, allowing the device to cool down. Once the device cools down by approximately 15°C, cycle the input voltage (below the UVLO falling threshold) to clear the fault latch and reactivate the device.

The thermal-overload protection protects the IC in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Design Procedure

Main Step-Up Regulator

Inductor Selection

The minimum inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output-load capability, transient-response time, and output-voltage ripple. Physical size and cost are also important factors to be considered.

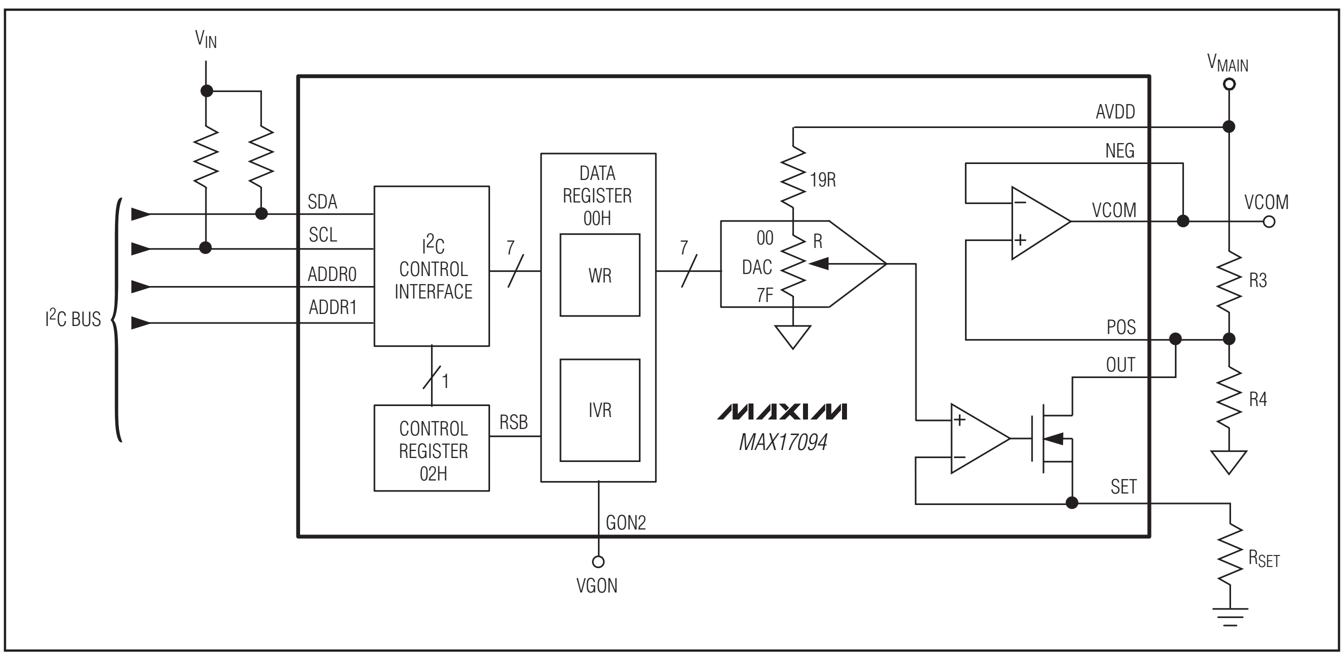


Figure 5. VCOM Calibrator Functional Diagram

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant called LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

In Figure 2's typical operating circuit, the LCD's gate-on and gate-off supply voltages are generated from two unregulated charge pumps driven by the step-up regulator's LX node. The additional load on LX must therefore be considered in the inductance and current calculations. The effective maximum output current, $I_{MAIN(EFF)}$, becomes the sum of the maximum load current of the step-up regulator's output plus the contributions from the positive and negative charge pumps:

$$I_{MAIN(EFF)} = I_{MAIN(MAX)} + n_{VN} \times I_{VN} + (n_{VP} + 1) \times I_{VP}$$

where $I_{MAIN(MAX)}$ is the maximum step-up output current, n_{VN} is the number of negative charge-pump stages, n_{VP} is the number of positive charge-pump stages, I_{VN} is the negative charge-pump output current, and I_{VP} is the positive charge-pump output current, assuming the initial pump source for I_{VP} is V_{MAIN}.

Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{MAIN(EFF)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics*, the desired switching frequency (f_{OSC}), and an estimate of LIR based on the above discussion:

$$L = \left(\frac{V_{IN}}{V_{MAIN}}\right)^2 \left(\frac{V_{MAIN} - V_{IN}}{I_{MAIN(EFF)} \times f_{OSC}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$ using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{MAIN(EFF)} \times V_{MAIN}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times \left(V_{MAIN} - V_{IN(MIN)}\right)}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX17094 LX current limit should exceed I_{PEAK} and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the typical operating circuit, the maximum load current ($I_{MAIN(MAX)}$) is 300mA, with an 8V output and a typical input voltage of 3.3V. The effective full-load step-up current is:

$$I_{MAIN(EFF)} = 300mA + 1 \times 20mA + (2 + 1) \times 20mA = 380mA$$

Choose a switching frequency of 1.2MHz and a LIR of 0.36, and estimate the efficiency to be 85% at this operating point:

$$L = \left(\frac{3.3V}{8V}\right)^2 \left(\frac{8V - 3.3V}{0.380A \times 1.2MHz}\right)\left(\frac{0.85}{0.36}\right) \approx 4.1\mu H$$

A 4.1µH inductor is chosen. Then, using the circuit's minimum input voltage (3.0V) and estimating efficiency of 82% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.38A \times 8V}{3V \times 0.82} \approx 1.24A$$

The ripple current and the peak current at that input voltage are:

$$I_{RIPPLE} = \frac{3V \times (8V - 3V)}{4.1\mu H \times 8V \times 1.2MHz} \approx 0.381A$$

$$I_{PEAK} = 1.24A + \frac{0.381A}{2} = 1.43A$$

Setting the Switching Frequency

To set the switching frequency, connect a resistor from FREQ to AGND. Calculate the resistor value in kΩ from the following equation:

$$f_{(MHZ)} = 0.015 \times R_{FREQ(k\Omega)}$$

Output Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}}\left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} f_{OSC}}\right)$$

and:

$$V_{RIPPLE(ESR)} \approx I_{PEAK} R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output-voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input Capacitor Selection

The input capacitor (C4) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. A 10µF ceramic capacitor is used in the typical operating circuit (Figure 2) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, C4 can be reduced below the values used in the typical operating circuit. Ensure a low noise supply at IN by using an adequate value for C4.

Rectifier Diode

The MAX17094's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 3A Schottky diode complements the internal MOSFET well.

Output-Voltage Selection

The output voltage of the main step-up regulator is adjusted by connecting a resistive voltage-divider from the output (V_{MAIN}) to AGND with the center tap connected to FB (see Figure 2). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{MAIN}}{1.235V} - 1\right)$$

where V_{REF}, the step-up regulator's feedback set point, is 1.235V (typical). Place R1 and R2 close to the IC.

Loop Compensation

Choose R_{COMP} to set the high-frequency integrator gain for fast-transient response. Choose C_{COMP} to set the integrator zero to maintain loop stability.

For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \approx \frac{250 \times V_{IN} \times V_{MAIN} \times C_{OUT}}{L \times I_{MAIN(MAX)}}$$

$$C_{COMP} \approx \frac{10 \times V_{MAIN} \times L \times I_{MAIN(MAX)}}{(V_{IN})^2 \times R_{COMP}}$$

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient-response waveforms.

Setting the LDO Output Voltage

The output voltage of the LDO is adjusted by connecting a resistive voltage-divider from the output (V_{LOUT}) to AGND with the center tap connected to FBL (see Figure 2). Select R8 in the 10kΩ to 50kΩ range. Calculate R7 with the following equation:

$$R7 = R8 \times \left(\frac{V_{LOUT}}{0.618V} - 1\right)$$

Place R7 and R8 close to the IC.

Connect to a 1µF capacitor between LIN and AGND to keep the source impedance to the LDO low and connect a 4.7µF low equivalent-series-resistance (ESR) capacitor between LOUT and AGND to ensure stability and to provide good output-transient performance.

Input-Voltage Detector

The falling-edge input-voltage threshold used by the voltage detector to drive YDCHG to VGON1 during power-down is adjusted by connecting a resistive voltage-divider from V_{IN} to AGND with the center tap connected to SENSE (see Figure 2). Select R6 in the 10kΩ range. Calculate R5 with the following equation:

$$R5 = R6 \times \left(\frac{V_{IN(THRESHOLD)}}{1.235V} - 1 \right)$$

Setting the VCOM Adjustment Range

The external resistive voltage-divider sets the maximum value of the VCOM adjustment range. R_{SET} sets the full-scale sink current, I_{OUT}, which determines the minimum value of the VCOM adjustment range. Large R_{SET} values increase resolution but decrease the VCOM adjustment range. Calculate R3, R4, and R_{SET} using the following procedure:

1) Choose the maximum VCOM level (V_{MAX}), the minimum VCOM level (V_{MIN}), and the AVDD supply voltage (V_{AVDD}).
2) Select R3 between 10kΩ and 500kΩ based on the acceptable power loss from the V_{MAIN} supply rail connected to AVDD.
3) Calculate R4:

$$R4 \cong \frac{V_{MAX}}{(V_{AVDD} - V_{MAX})} \times R3$$

4) Calculate R_{SET}:

$$R_{SET} = \frac{V_{MAX}}{20 \times (V_{MAX} - V_{MIN})} \times R3$$

5) Verify that I_{SET} does not exceed 120µA:

$$I_{SET} = \frac{V_{AVDD}}{20 \times R_{SET}}$$

6) If I_{SET} exceeds 120µA, return to step 2 and choose a larger value for R1.

   The resulting resolution is:

$$\frac{(V_{MAX} - V_{MIN})}{127}$$

A complete design example is given below:

V_{MAX} = 4V, V_{MIN} = 2.4V, V_{MAIN} = 8V

If R3 = 200kΩ, then R4 = 200kΩ and R_{SET} = 24.9kΩ.

Resolution = 12.5mV

Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow.

The MAX17094, with its exposed backside paddle soldered to $1in^2$ of PCB copper, can dissipate about 2222mW into +70°C still air. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability. The major components of power dissipation are the power dissipated in the step-up regulator and the power dissipated by the operational amplifiers.

The MAX17094's largest on-chip power dissipation occurs in the step-up switch, the VCOM amplifiers, the LDO, and the high-voltage scan driver outputs.

Step-Up Regulator

The largest portions of the power dissipated by the step-up regulator are the internal MOSFET, the inductor, and the output diode. If the step-up regulator with 3.3V input and 300mA output has approximately 85% efficiency, approximately 5% of the power is lost in the internal MOSFET, approximately 3% in the inductor, and approximately 5% in the output diode. The remaining few percent are distributed among the input and output capacitors and the PCB traces. If the input power is approximately 3W, the power lost in the internal MOSFET is approximately 150mW.

Operational Amplifiers

The power dissipated in the operational amplifiers depends on the output current, the output voltage, and the supply voltage:

$$PD_{SOURCE} = I_{VCOM\_SOURCE} \times (V_{AVDD} - V_{VCOM})$$

$$PD_{SINK} = I_{VCOM\_SINK} \times V_{VCOM}$$

where I_{VCOM_SOURCE} is the output current sourced by one operational amplifier, and I_{VCOM_SINK} is the output current that the operational amplifier sinks.

In a typical case where the supply voltage is 8V and the output voltage is 4V with an output source current of 30mA for each of the four operational amplifiers, the power dissipated is 480mW.

LDO

The power dissipated in the LDO depends on the LDO's output current, input voltage, and output voltage:

$$PD_{LDO} = I_{LOUT} \times (V_{LIN} - V_{LOUT})$$

Scan Driver Outputs

The power dissipated by the scan driver outputs (Y2–Y8) depends on the scan frequency, the voltage difference between the power rails across each driver, and the capacitive load driven by each output. Assuming the voltage difference between the power rails of each driver is 30V and all outputs are driving a load capacitance of 4nF at 50kHz, then the total expected power dissipation would be:

$$PD_{SCAN} = 7 \times f_{SCAN} \times C_{PANEL} \times (V_{GON\_} - V_{GOFF})^2$$
$$= 7 \times 50kHz \times 4nF \times (30V)^2 = 1.26W$$

VCOM Calibrator Interface

The MAX17094 is a slave-only device. The 2-wire I²C-bus-like serial interface (pins SCL and SDA) is designed to attach to an I²C bus that is pulled up to V_{IN}. Connect both SCL and SDA lines to the I²C bus supply through individual pullup resistors. Calculate the required value of the pullup resistors using:

$$R_{PULLUP} \le \frac{t_R}{C_{BUS}}$$

where t_R is the rise time in the *Electrical Characteristics*, and C_{BUS} is the total capacitance on the bus.

The MAX17094 uses a nonstandard I²C interface protocol with standard voltage and timing parameters, as defined in the following subsections.

Bus Not Busy

Both data and clock lines remain high. Data transfers can be initiated only when the bus is not busy (Figure 6).

Start Data Transfer (S)

Starting from an idle bus state (both SDA and SCL are high), a high-to-low transition of the SDA line while the clock (SCL) is high determines a START condition. All commands must be preceded by a START condition from a master device on the bus.

Stop Data Transfer (P)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a STOP condition. All operations must be ended with a STOP condition from the master device.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. The master generates one clock pulse per bit of data during write operations and the slave device outputs 1 data bit per clock pulse during read operations. Each data transfer is initiated with a START condition and terminated with a STOP condition. Two bytes are transferred between the START and STOP conditions.

Acknowledge/Polling

The MAX17094, when addressed, generates an acknowledge pulse after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. The master signals an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

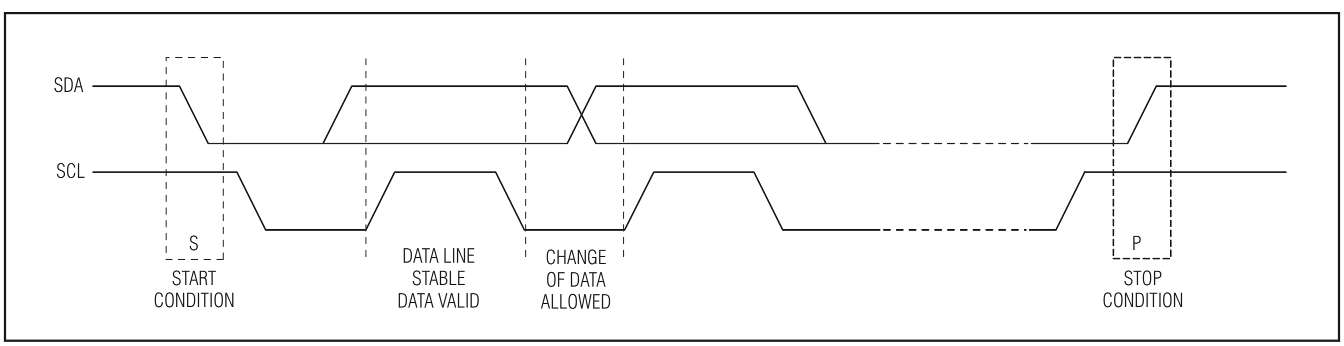


Figure 6. I²C Bus START, STOP, and Data Change Conditions

The MAX17094 does not generate an acknowledge while an internal programming cycle is in progress. Once the internally timed write cycle has started and the IVR inputs are disabled, acknowledge polling can be initiated. This involves sending a START condition followed by the device address byte. Only if the internal write cycle has completed does the MAX17094 respond with an acknowledge pulse, allowing the read or write sequence to continue.

The MAX17094 does not acknowledge a command to program IVR if V_{GON} is not high enough to properly program the device. Also, a program command must be preceded by a write command. The IC does not acknowledge a program command or program IVR unless the WR data has been modified since the most recent program command.

Address Byte and Address Pins

The MAX17094's slave address is determined by the state of the A0 and A1 address pins. These pins allow up to four devices to reside on the same I^2C bus. Address pins tied to AGND result in a 0 in the corresponding bit position in the slave address. Conversely, address pins tied to V_{IN} result in a 1 in the corresponding bit positions. For example, the MAX17094's slave address byte is 50h when A0 and A1 pins are grounded (see Figure 8).

Registers

The MAX17094 contains two user-accessible registers: the data register located at 00h and the access control register (ACR) located at 02h.

Data Register 00h

The data register contains the WR value that directly determines the wiper position of the potentiometer, and the IVR value stored in the nonvolatile memory, which is used to preset the WR during power-up. The status of the ACR determines whether WR and/or IVR is accessed during read and write operations involving the data register (see the *Access Control Register (ACR) 02h* section). When reading and writing to the data register, the most significant bit (MSB) is ignored. Figure 9 shows the data register byte.

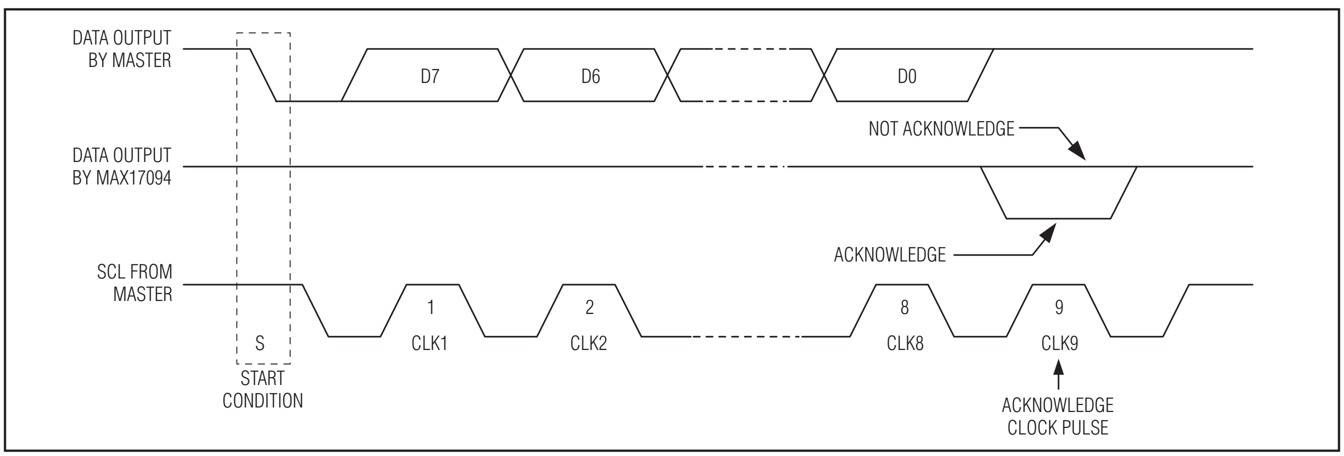


Figure 7. I^2C Bus Acknowledge

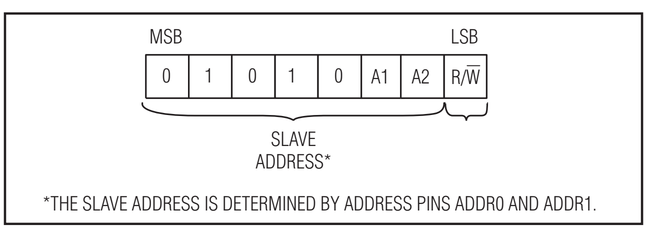


Figure 8. Address Byte

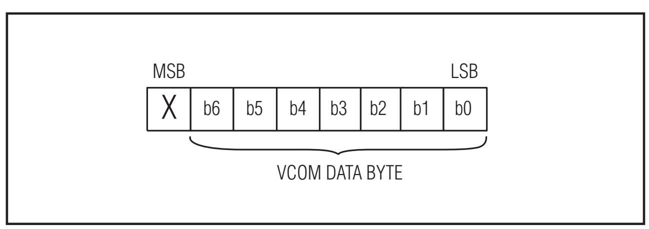


Figure 9. Data Register Byte

Table 3 lists the WR values and the corresponding I_{SET}, V_{SET}, and V_{OUT} values.

Access Control Register (ACR) 02h

The register select bit (RSB) is the most significant bit of the byte stored in the ACR and is used to select whether WR or IVR is accessed during read and write cycles involving the data register.

When writing to the data register, if RSB is set to 1, only WR is updated with the value written to the data register. If RSB is set to 0, both WR and IVR are updated with the value written that was written to the data register.

When reading the data register, if RSB is set to 1, the value read from the data register is from WR: otherwise, if RSB is set to 0, the value read from the data register is from IVR.

When configuring RSB, only 00h or 80h should be written to the ACR to set RSB to 0 or 1, respectively, in order to keep all bits other than the RSB bit in the ACR to zeros. The ACR comprises volatile memory, which is preset to 00h during power-up. Figure 10 shows the ACR byte.

Table 3. DAC Settings

7-BIT VCOM DATA BYTE	I_{SET}	V_{SET} (V)	V_{OUT} (V)
0000000	$I_{SET(MAX)}$	$V_{SET(MAX)}$	V_{MIN}
0000001	$I_{SET(MAX)}$ - 1 LSB	$V_{SET(MAX)}$ - 1 LSB	V_{MIN} + 1 LSB
. . .	. . .	. . .	. . .
1111110	$I_{SET(MIN)}$ + 1 LSB	$V_{SET(MIN)}$ + 1 LSB	V_{MAX} - 1 LSB
1111111	$I_{SET(MIN)}$	$V_{SET(MIN)}$	V_{MAX}

Write Operation

To perform a write operation, the master must generate a START condition, write the slave address byte (R/W = 0), write the register address, write the byte of data, and generate a STOP condition. When writing to the WR/IVR register, the potentiometer adjusts to the new setting once it has acknowledged the new data has been written to WR. If the ACR is set such that both WR and IVR are to be updated with the value written to the WR/IVR register, a write cycle is performed first to update WR, followed by an internal write cycle to update IVR. The SCL and SDA lines are ignored until the internal IVR write cycle has finished. Figure 11 shows the write operation.

Read Operation

To perform a read operation, the master generates a START condition, writes the slave address byte (R/W = 0), writes the register address, generates a repeated START condition, writes the slave address byte (R/W = 1), reads data with ACK or NACK as applicable, and generates a STOP condition. Figure 12 shows a read operation.

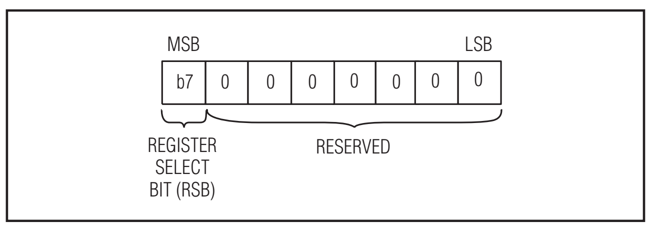


Figure 10. Access Control Register Byte

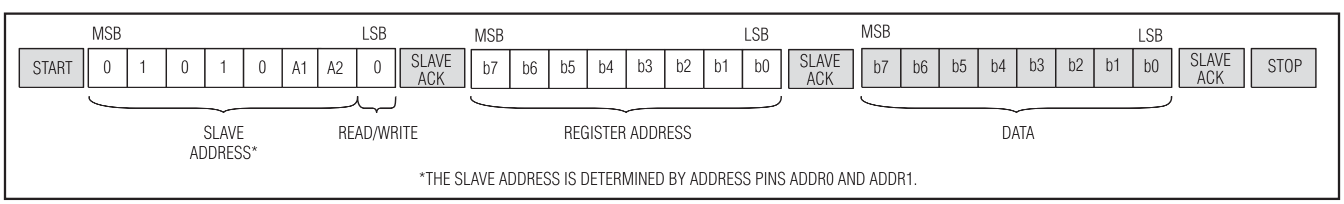


Figure 11. Write Operation

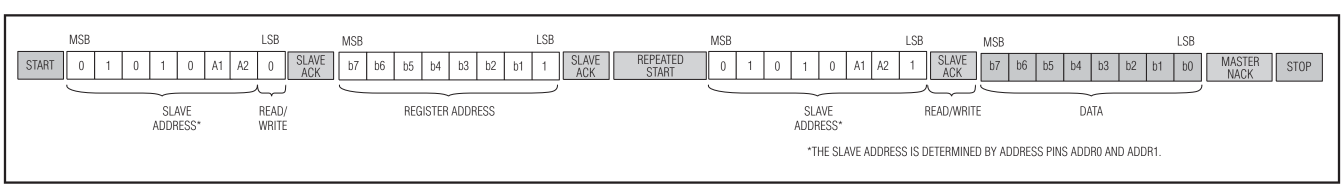


Figure 12. Read Operation

Internal-Switch Boost Regulator with Integrated 7-Channel Driver, VCOM Calibrator, Op Amp, and LDO

PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Minimize the area of high-current loops by placing the inductor, output diode, and output capacitors near the input capacitors and near the LX and PGND pins. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pin, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D1), to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
- Create a power ground island (PGND) consisting of the input and output capacitor grounds, PGND pin, and any charge-pump components. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output-voltage ripple and noise spikes. Create an analog ground plane (AGND) consisting of the AGND pin, all the feedback-divider ground connections, the operational-amplifier-divider ground connections, the COMP capacitor ground connection, the AVDD capacitor ground connection, and the device's exposed backside pad. Create a ground plane (BGND) to carry operational amplifier return current with the AVDO bypass capacitor connected to this ground plane. Connect the AGND, BGND, and PGND islands by connecting the PGND and BGND pins directly to the exposed backside pad. Make no other connections between these separate ground planes.
- Place the feedback-voltage-divider resistors as close to the feedback pin as possible. The divider's center trace should be kept short. Placing the resistors far away causes the FB trace to become an antenna that can pick up switching noise. Care should be taken to avoid running the feedback trace near LX or the switching nodes in the charge pumps.
- Place IN pin bypass capacitors as close to the device as possible. The ground connections of the IN bypass capacitor should be connected directly to the AGND pin with a wide trace.
- Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
- Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from the feedback node and analog ground. Use DC traces as shields, if necessary.

Refer to the MAX17094 evaluation kit for an example of proper board layout.

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 TQFN	T4866N+1	21-0141

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