

PI74ALVCH16721

3.3V 20-Bit Flip-Flop with 3-STATE Outputs

Product Features

- PI74ALVCH16721 is designed for low voltage operation
- $V_{CC} = 2.3 V$ to 3.6V
- Hysteresis on all inputs
- Typical V_{OLP} (Output Ground Bounce) < 0.8V at V_{CC} = 3.3V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) < 2.0V at V_{CC} = 3.3V, T_A = 25°C
- Bus Hold retains last active bus state during 3-STATE, eliminating the need for external pullup resistors
- Industrial operation at -40°C to +85°C
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A)
 - 56-pin 300 mil wide plastic SSOP (V)

Product Description

Pericom Semiconductor's PI74ALVCH series of logic circuits are produced in the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

The PI74ALVCH16721 is a 20-bit flip-flop with 3-state outputs designed specifically for 2.3V to 3.6V V_{CC} operation. The PI74ALVCH16721 is designed with edge-triggered D-type flip-flops with qualified clock storage. On the positive transition of clock (CLK) input, the device provides true data at the Q outputs, provided that the clock-enable (CLKEN) input is LOW. If CLKEN is HIGH, no data is stored.

A buffered output-enable (\overline{OE}) input can be used to place the 20 outputs in either a normal logic state (HIGH or LOW level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capacity to drive bus lines without the need for interface or pullup components. \overline{OE} does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overrightarrow{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The PI74ALVCH16721 data has "Bus Hold" which retains the data input's last state whenever the data input goes to high-impedance preventing "floating" inputs and eliminating the need for pullup/down resistors.



Logic Block Diagram

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PI74ALVCH16721 3.3V 20-Bit Flip-Flop with 3-State Outputs

Product Pin Description

Pin Name	Description
ŌĒ	Output Enable Input (Active LOW)
CLKEN	Clock Enable Input (Active LOW)
CLK	Clock Input (Active HIGH)
Dx	Data Inputs
Qx	3-State Outputs
GND	Ground
V _{CC}	Power

Product Pin Configuration

$ \overrightarrow{OE} \ \ \ 1 \\ Q1 \ \ \ 2 \\ Q2 \ \ \ 3 \\ GND \ \ \ 4 \\ Q3 \ \ \ 5 \\ Q4 \ \ \ \ 6 \\ VCC \ \ \ \ 7 \\ Q5 \ \ \ \ 8 \\ Q6 \ \ \ \ 9 \\ Q7 \ \ \ \ \ 10 \\ GND \ \ \ \ \ 11 \\ Q8 \ \ \ \ \ 12 \\ Q9 \ \ \ \ \ 13 \\ Q10 \ \ \ \ \ 11 \\ Q8 \ \ \ \ \ \ 12 \\ Q9 \ \ \ \ \ 13 \\ Q10 \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	56 CLK 55 D1 54 D2 53 GND 52 D3 51 D4 50 VCC 49 D5 48 D6 47 D7 46 GND 45 D8 44 D9 43 D10 42 D11 41 D12 40 D13 39 GND 38 D14 37 D15 36 D16 35 VCC 34 D17
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	43 D10 42 D11 41 D12 40 D13
Q14 [19 Q15 [20 Q16 [21 VCC [22	38
Q17 [23 Q18 [24 GND [25 Q19 [26 Q20 [27 NC [28	33] D18 32] GND 31] D19 30] D20 29] CLKEN

Truth Table⁽¹⁾

	Outputs			
ŌĒ	CLKEN	CLK	Dx	Qx
L	Н	Х	Х	Q0
L	L	↑	Н	Н
L	L	↑	L	L
L	L	L or H	Х	Q ₀
Н	Х	Х	Х	Z

Notes:

1. H = High Signal Level

L = Low Signal Level

X = Don't Care or Irrelevant

Z = High Impedance

 \uparrow = LOW-to-HIGH Transition



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature65°C to +150°C
Ambient Temperature with Power Applied40°C to +85°C
Input Voltage Range, V_{IN} 0.5V to V_{CC} +0.5V
Output Voltage Range, V _{OUT}
DC Input Voltage0.5V to +5.0V
DC Output Current 100 mA
Power Dissipation 1.0W

Note:

Stresses greater than those listed under MAXIMUM RAT-INGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^{\circ}$ C to $+85^{\circ}$ C, $V_{CC} = 3.3V \pm 10\%$)

Parameters	s Description Test Conditions ⁽¹⁾		Min.	Тур. ⁽²⁾	Max.	Units			
V _{CC}	Supply Voltage		2.3		3.6				
V _{IH} ⁽³⁾		$V_{CC} = 2.3 V$ to 2.7V	1.7			1			
	Input HIGH Voltage	$V_{CC} = 2.7 V$ to 3.6V	2.0			-			
V _{IL} ⁽³⁾		$V_{CC} = 2.3 V$ to 2.7 V			0.7				
VII.(-)	Input LOW Voltage	$V_{\rm CC} = 2.7 V$ to 3.6V			0.8				
V _{IN} ⁽³⁾	Input Voltage		0		V _{CC}				
V _{OUI} ⁽³⁾	Output Voltage		0		V _{CC}				
		I_{OH} = -100µA, V_{CC} = Min. to Max.	V _{CC} -0.2						
		$V_{IH} = 1.7V, I_{OH} = -6mA, V_{CC} = 2.3V$	2.0			V			
V _{OH}	Output HIGH Voltage	V_{IH} = 1.7V, I_{OH} = -12mA, V_{CC} = 2.3V	1.7						
- OII		$V_{IH} = 2.0V, I_{OH} = -12mA, V_{CC} = 2.7V$	2.2						
		$V_{IH} = 2.0V, I_{OH} = -12mA, V_{CC} = 3.0V$	2.4						
		$V_{IH} = 2.0V, I_{OH} = -24mA, V_{CC} = 3.0V$	2.0						
	Output LOW Voltage	$I_{OL} = 100 \mu A$, $V_{IL} =$ Min. to Max.			0.2				
		$V_{IL} = 0.7V$, $I_{OL} = 6mA$, $V_{CC} = 2.3V$			0.4				
V _{OL}		$V_{IL} = 0.7V$, $I_{OL} = 12mA$, $V_{CC} = 2.3V$			0.7				
		$V_{IL} = 0.8V$, $I_{OL} = 12mA$, $V_{CC} = 2.7V$	$V_{\rm IL} = 0.8 \text{V}, \ \text{I}_{\rm OL} = 12 \text{mA}, \ \text{V}_{\rm CC} = 2.7 \text{V}$ (6)						
		$V_{IL} = 0.8V$, $I_{OL} = 24mA$, $V_{CC} = 3.0V$			0.55				
	Output HIGH Current	$V_{CC} = 2.3 V$			-12				
I _{OH} ⁽³⁾		$V_{CC} = 2.7 V$	V _{CC} = 2.7V		-12				
		$V_{CC} = 3.0V$			-24				
	Output	$V_{CC} = 2.3 V$			12	mA			
I _{OL} ⁽³⁾	LOW Current	$V_{\rm CC} = 2.7 V$		12					
		$V_{CC} = 3.0 V$			24				



Parameters	Description	Test Conditions ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units			
I _{IN}	Input Current	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.6V$			± 5	,			
		$V_{IN} = 0.7V, V_{CC} = 2.3V$	45						
	Input	$V_{IN} = 1.7V, V_{CC} = 2.3V$	-45						
$I_{\mathbb{IN}}$ (hold)	Hold Current	$V_{IN} = 0.8V, V_{CC} = 3.0V$	75						
	Current	$V_{IN} = 2.0V, V_{CC} = 3.0V$	-75						
		$V_{IN} = 0$ to 3.6V, $V_{CC} = 3.6V$			±500	μΑ			
I _{OZ}	Output Current (3-STATE Outputs)	$V_{OUT} = V_{CC}$ or GND, $V_{CC} = 3.6V$			±10				
I _{CC}	Supply Current	$V_{CC} = 3.6V, I_{OUT} = 0\mu A,$ $V_{IN} = GND \text{ or } V_{CC}$			40				
ΔI _{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = 3.0V$ to $3.6V$ One Input at $V_{CC} - 0.6V$ Other Inputs at V_{CC} or GND			750				
CI	Control Inputs			3					
	Data Inputs	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.3V$		6		pF			
CO	Outputs	$V_{\rm O} = V_{\rm CC}$ or GND, $V_{\rm CC} = 3.3$ V		7					

DC Electrical Characteristics-Continued (Over the Operating Range, $T_A = -40^{\circ}$ C to $+85^{\circ}$ C, $V_{CC} = 3.3V \pm 10\%$)

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at $V_{CC} = 3.3V$, $+25^{\circ}C$ ambient and maximum loading.

3. Unused Control Inputs must be held HIGH or LOW to prevent them from floating.



Switching Characteristics over Operating Range⁽¹⁾

D (Description Conditions ⁽		$V_{\rm CC} = 2.5 V \pm 0.2 V$		$V_{\rm CC} = 2.7 V$		$V_{\rm CC} = 3.3 \mathrm{V} \pm 0.3 \mathrm{V}$		U
Parameters		Conditions	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Units
fclock	Clock Frequency		0	150	0	150	0	150	MII-
f _{MAX}	Maximum Frequency		150		150		150		MHz
tplh, tphl	Propogation Delay CLK to Qx	$C_L = 50 pF$ $R_L = 500 \Omega$		5.6		5.1		4.3	
tpzH, tpzL	Output Enable Time OE to Qx		1.0	6.1	1.0	5.8	1.0	4.8	
tPHX	Output Disable Time \overline{OE} to Qx			5.5		4.7		4.4	
t _{SU}	Data Before CLK↑		4		3.6		3.1		ns
t _{SU}	CLKEN Before CLK↑		3.4		3.1		2.7		
t _H	Data After CLK↑		0		0		0		
t _H	CLKEN After CLK↑	-	0		0		0		
tw	Pulse Width ⁽³⁾ CLK HIGH or LOW		3.3		3.3		3.3		
$\Delta t / \Delta v^{(4)}$	Input Transition RISE	or FALL	0	10	0	10	0	10	ns/V

Notes:

1. See test circuit and waveforms.

2. Minimum limits are guaranteed but not tested on Propagation Delays.

3. Recommended operating condition.

Operating Characteristics, $T_A = 25^{\circ}C$

Parameter		Test Conditions	The set Conditions $\frac{V_{CC} = 2.5V \pm 0.2V}{Typ}.$		Units
		Test Conditions			Units
CPD Power Dissipation	Outputs Enabled	$C_{L} = 50 \text{pF}, \text{ f} = 10 \text{ MHz}$	55	59	рF
Capacitance	Outputs Disabled	$C_{\rm L} = 30 \text{pr}, 1 = 10 \text{ MHz}$	46	49	pr

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