MAX3522B DOCSIS 3.1 Programmable-Gain Amplifier

General Description

The MAX3522B is a programmable gain amplifier (PGA) designed to exceed the DOCSIS 3.1 Upstream Transmit requirements. By providing dual outputs, the MAX3522B eliminates the need for an external RF switch when selecting between two different upstream bandwidths. The PGA meets the DOCSIS 3.1 spurious limits while transmitting a combined output power of 68dBmV over the RF bandwidth of 5MHz to 204MHz from either output. The gain is controlled in 1dB steps over a 54dB range using a SPI 3-wire interface. The use of Maxim's high-voltage CMOS process enables the device to deliver high dynamic range, while minimizing power dissipation under a +5V supply rail.

The MAX3522B is available in a 56-pin 8mm x 8mm x 0.75mm TQFN package, and operates over temperature range of 0°C to +70°C.

Applications

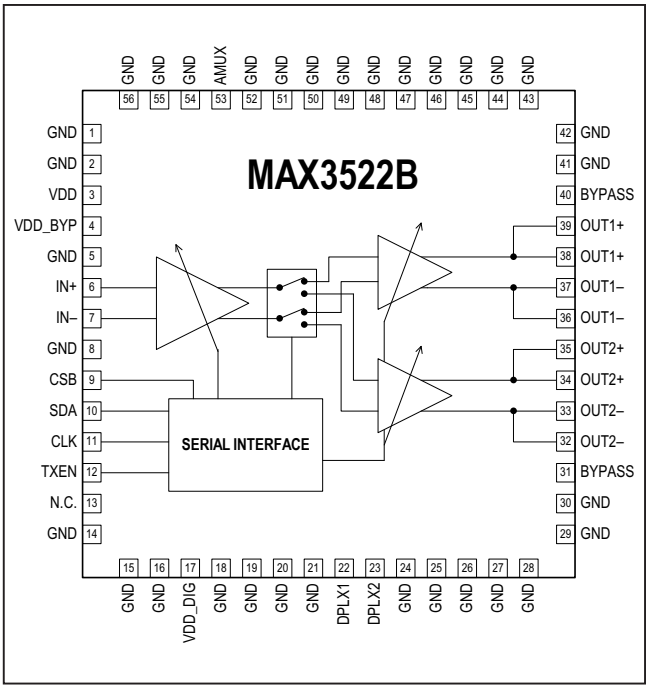
- DOCSIS 3.1 Upstream (D3.1 US)
- Cable Modem (CM)
- Customer Premises Equipment (CPE)

Benefits and Features

- Delivers +68dBmV Output Power While Meeting DOCSIS 3.1 Requirements
- Covers 5MHz–204MHz Output Bandwidth
- Dual Outputs Eliminates Need for an External RF Switch
- Programmable Power Codes Allow Operation at Reduced Power Dissipation
- Exceeds Spurious Requirements with Fully Loaded OFDM Allocation at +65dBmV at Modem Output
- Two GPIO's Available for SPI-bus Control of External RF Switches
- 56L 8mm x 8mm x 0.75mm TQFN Package with Exposed Paddle

Ordering Information *appears at end of data sheet.*

Simplified Block Diagram



19-100012; Rev 0; 6/17

maxim integrated™

Absolute Maximum Ratings

VDD, VDD_BYP, VDD_DIG to GND .....-0.3V to +5.5V
TXEN, SDA, SCLK, CSB .....-0.3V to +4.2V
IN+, IN-.....-0.3V to V_{DD} + 0.3V
OUT1+, OUT1-, OUT2+, OUT2- to GND.....-0.3V to V_{DD} + 3V
RF Input Power .....+10dBm
Continuous Power Dissipation (T_A = 70°C) (derate 100mW/°C above T_A = 70°C).....6037.5mW
Operating Temperature Range (100% duty-cycle)...0°C to 70°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

Package Information

56L TQFN Sawn

PACKAGE CODE	T5688+2
Outline Number	21-0135
Land Pattern Number	90-0046
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	PCB board must be designed for a θ_{JA} of 10°C/W or lower
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = 4.75V to 5.25V, V_{GND} = 0V, Z_{OUT} = 75Ω, TXEN = high, Power code = 3, T_A = 0°C to 70°C, Typical values are at V_{DD} = 5V, T_A = +25°C, unless otherwise noted. *Typical Application Circuit* as shown. Note 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Transmit Mode	I_{DD}	Gain code = 63, power code = 1		725		mA
		Gain code = 63, power code = 2		870		
		Gain code = 63, power code = 3, T_A = 70°C		1100	1150	
Supply Current Transmit Disable Mode	I_{DD}	TXEN = low		2.5	3.3	mA
Input High Voltage	V_{INH}		2		3.6	V
Input Low Voltage	V_{INL}				0.7	V
Input High Current	I_{BIASH}				10	µA
Input Low Current	I_{BIASL}		-10			µA
GPIO Output Voltage		3mA sink current			0.4	V
GPIO Input Current		High impedance	-10		+10	µA
AC ELECTRICAL SPECIFICATIONS						
Voltage Gain, Z_{IN} = 100Ω (Note 3), Power Code = 3, F_{IN} = 10MHz	A_V	Gain code = 63 (Note 2)	24.2	25.2	26.2	dB
		Gain code = 53 (Note 2)	14.7	15.7	16.7	
		Gain code = 43 (Note 2)	5.2	6.2	7.2	
		Gain code = 33 (Note 2)	-4.6	-3.6	-2.6	
		Gain code = 23 (Note 2)	-14.3	-13.3	-12.3	
		Gain code = 13 (Note 2)	-24.3	-23.3	-22.3	
Voltage Gain Variation with Power Code, Any Gain Code	Δ_{AV}			±0.1		dB
Gain Rolloff		Voltage gain = -28dB to +25dB, f_{IN} = 5MHz to 204MHz		-0.3		dB
Gain Step Size		Voltage gain = -28dB to +25dB, f_{IN} = 10MHz		1		dB
Transmit-Disable Mode Noise		BW = 160kHz, 5MHz to 204MHz, TXEN = low, voltage gain = -24dB to +25B		-66		dBmV
Isolation in Transmit-Disable Mode		TXEN = low		80		dB
Noise Figure	NF	Transmit mode, voltage gain = -1dB to +25dB		12		dB
Noise Figure Slope		Transmit mode, voltage gain = -28dB to +25dB		-1		dB/dB
DOCSIS 3.1 SNR	SNR	5 - 204MHz DOCSIS 3.1 OFDM channel, P_{OUT} = +68dBmV		60		dB
Transmit-Disable/Transmit-Enable Transient Duration		TXEN input rise/fall time < 0.1µs		4		µs
Transmit-Disable/Transmit-Enable Transient Amplitude		Gain = 25dB		20	50	mV_{PP}
		Gain = 4dB		1		mV_{PP}
Input Impedance	Z_{IN}	Balanced (Note 3)		200		Ω
Output Return Loss	S22	5 - 204MHz, TXEN = high (Note 4)		14		dB
Output Return Loss in Transmit-Disable Mode	S22	5 - 204MHz, TXEN = low (Note 4)		14		dB

Electrical Characteristics (continued)

(V_{DD} = 4.75V to 5.25V, V_{GND} = 0V, Z_{OUT} = 75Ω, TXEN = high, Power code = 3, T_A = 0°C to 70°C, Typical values are at V_{DD} = 5V, T_A = +25°C, unless otherwise noted. *Typical Application Circuit* as shown. Note 1.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
2nd Harmonic	HD2	f_{IN} = 100MHz, V_{OUT} = +68dBmV (Note 2)			-55		dBc
Two-Tone 2nd-Order Distortion (f_1 + f_2)	IM2	f_1 = 75MHz, f_2 = 80MHz, V_{OUT} = +65dBmV/tone (Note 2)			-55		dBc
3rd Harmonic Distortion	HD3	f_{IN} = 65MHz, V_{OUT} = +68dBmV (Note 2)			-60	-55	dBc
Two-Tone 3rd-Order Distortion	IM3	f_1 = 75MHz, f_2 = 80MHz, V_{OUT} = +65dBmV/tone			-63	-57	dBc
Output Compression at Peak Output		Gain = 25dB, output power = +79dBmV			0.3		dBmV
MER		4k FFT, 1024-QAM, V_{OUT} = +66dBmV	f_{IN} = 150MHz, BW = 96MHz		48.5		dB
			f_{IN} = 192MHz, BW = 24MHz		47		
		4k FFT, 1024-QAM, V_{OUT} = +67dBmV, L1 = L2 = 68nH, C14 = C15 = 10pF	f_{IN} = 150MHz, BW = 96MHz		46.4		
			f_{IN} = 192MHz, BW = 24MHz		47.3		
SERIAL PROGRAMMABLE INTERFACE							
CSB to SCLK Rise Setup Time	t_{SENS}				20		ns
CSB to SCLK Rise Hold Time	t_{SENH}				10		ns
SDA to SCLK Setup Time	t_{SDAS}				20		ns
SDA to SCLK Hold Time	t_{SDAH}				10		ns
SCLK Pulse-Width High	t_{SCLKH}				50		ns
SCLK Pulse-Width Low	t_{SCLKL}				50		ns
Maximum SCLK Frequency	f_{SCLK}			10			MHz

Note 1: Limits are tested at T_A = +70°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Guaranteed by design and characterization.

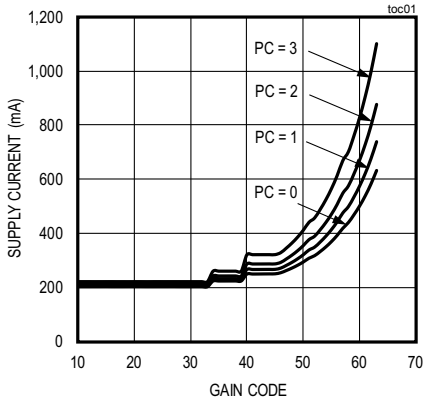
Note 3: For operation from a 100Ω source impedance, a 200Ω external shunt resistance must be added. See *Typical Application Circuit*.

Note 4: Output return loss is measured with the LC matching network, as shown in the *Typical Application Circuit*.

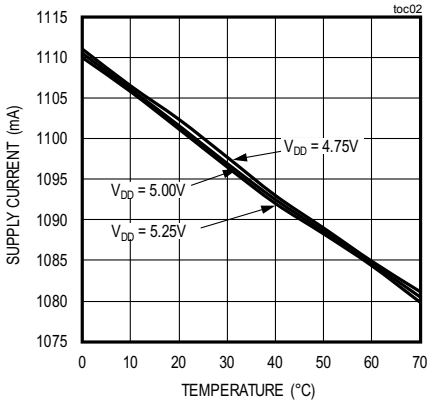
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

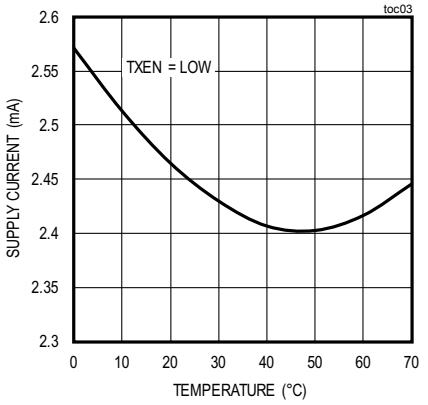
SUPPLY CURRENT vs. GAIN CODE



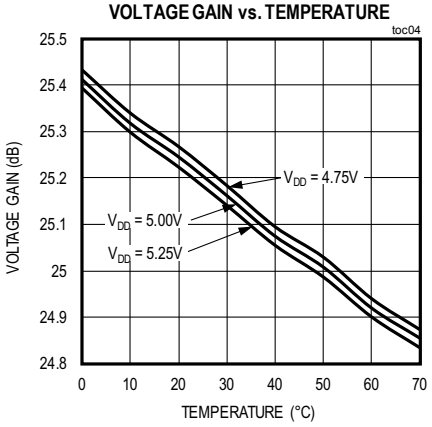
SUPPLY CURRENT vs. TEMPERATURE



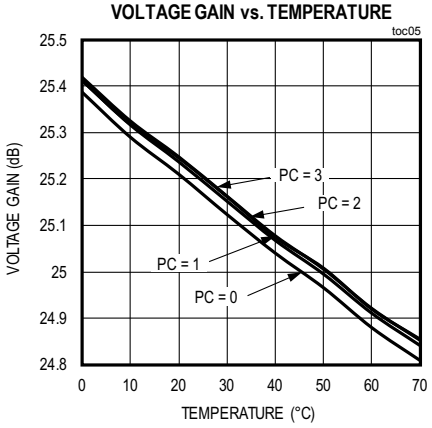
TRANSMIT-DISABLE CURRENT vs. TEMPERATURE



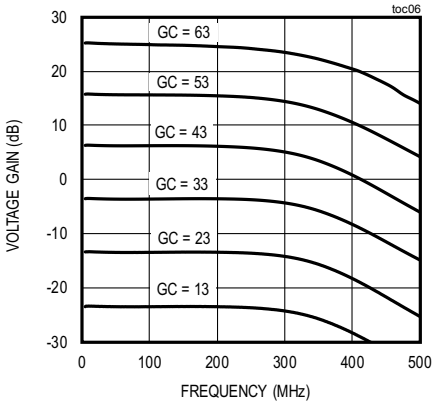
VOLTAGE GAIN vs. TEMPERATURE



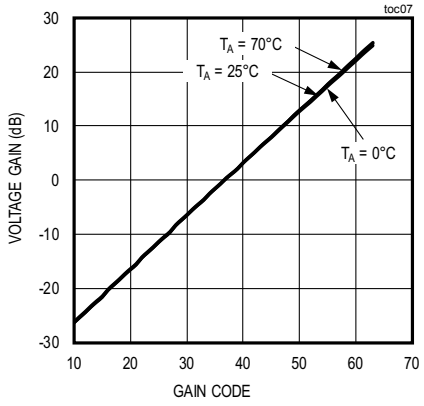
VOLTAGE GAIN vs. TEMPERATURE



VOLTAGE GAIN vs. FREQUENCY



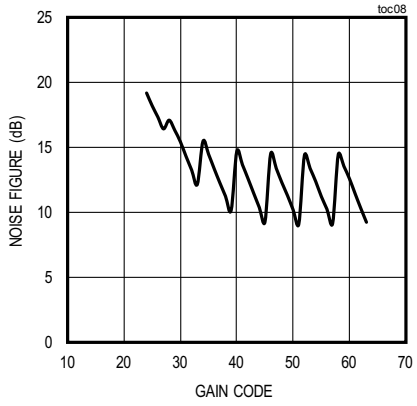
VOLTAGE GAIN vs. GAIN CODE



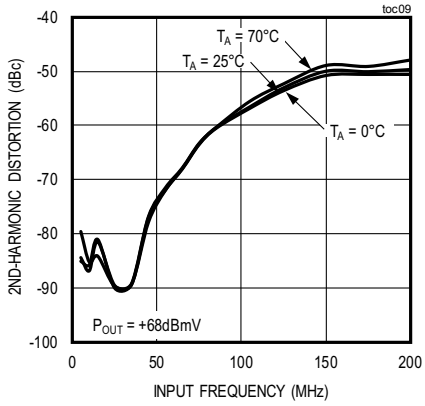
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

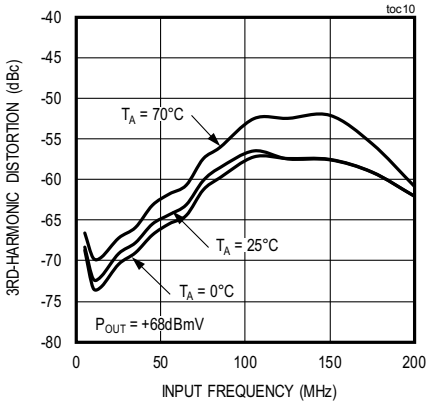
NOISE FIGURE vs. GAIN CODE



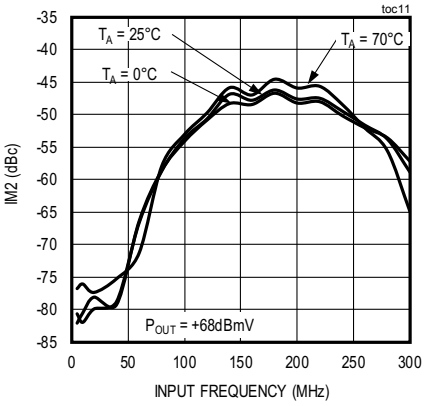
2ND-HARMONIC DISTORTION vs. INPUT FREQUENCY



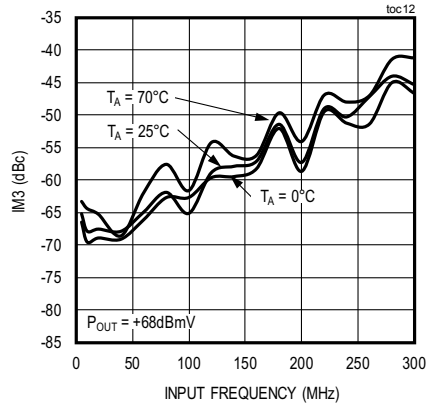
3RD-HARMONIC DISTORTION vs. INPUT FREQUENCY



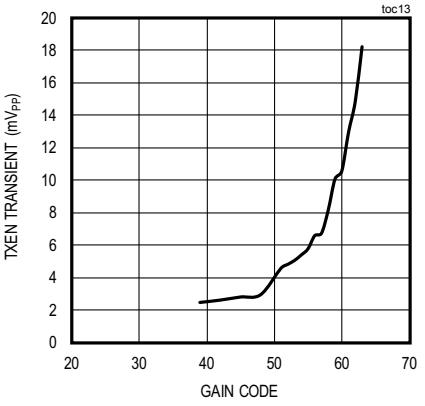
IM2 vs. INPUT FREQUENCY ($f_1 + f_2$)



IM3 vs. INPUT FREQUENCY



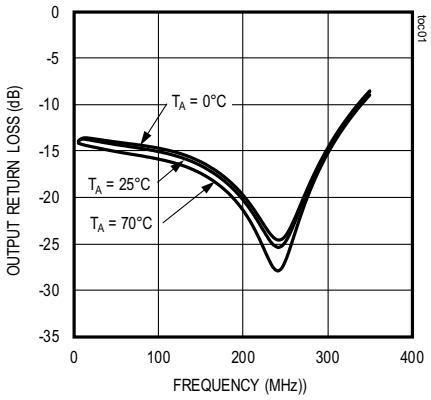
TXEN TRANSIENT vs. GAIN CODE



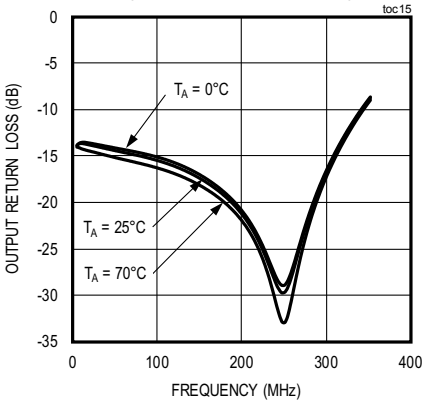
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

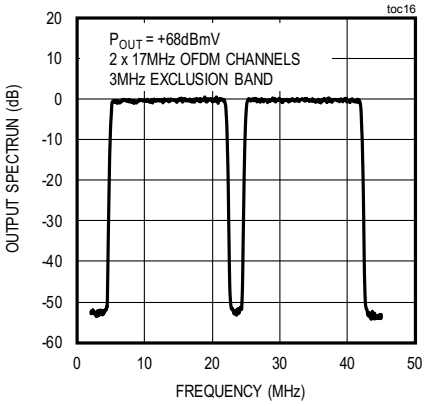
OUTPUT RETURN LOSS vs. FREQUENCY



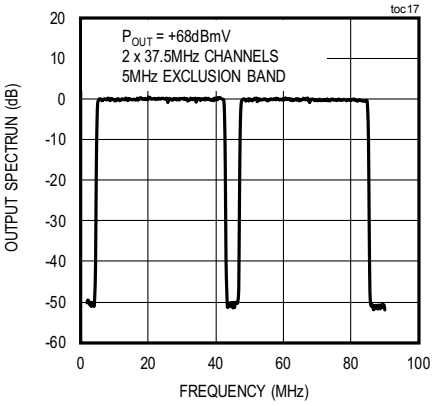
OUTPUT RETURN LOSS vs. FREQUENCY (TRANSMIT DISABLE MODE)



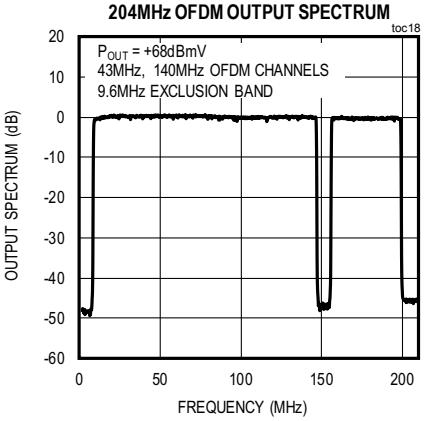
42MHz OFDM OUTPUT SPECTRUM



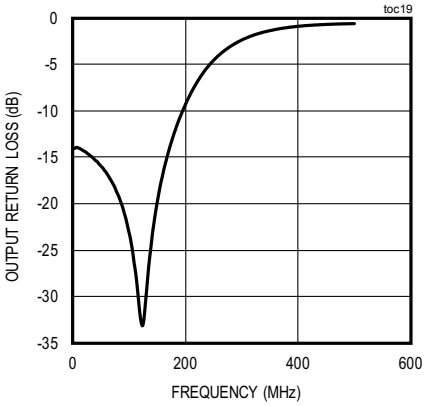
85MHz OFDM OUTPUT SPECTRUM



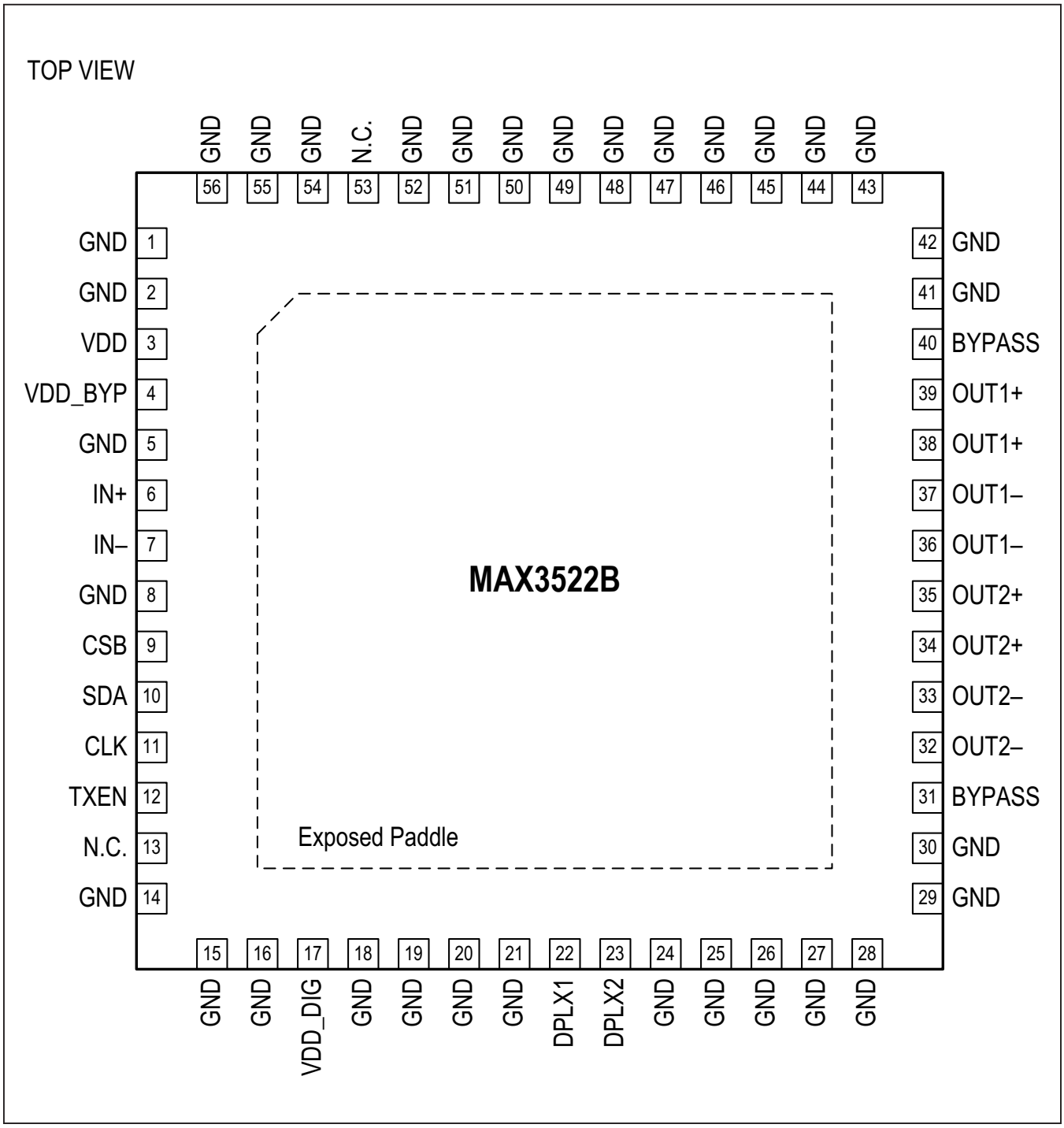
204MHz OFDM OUTPUT SPECTRUM



OUTPUT RETURN LOSS vs. FREQUENCY (L1 = L2 = 68nH, C14 = C15 =10pF)



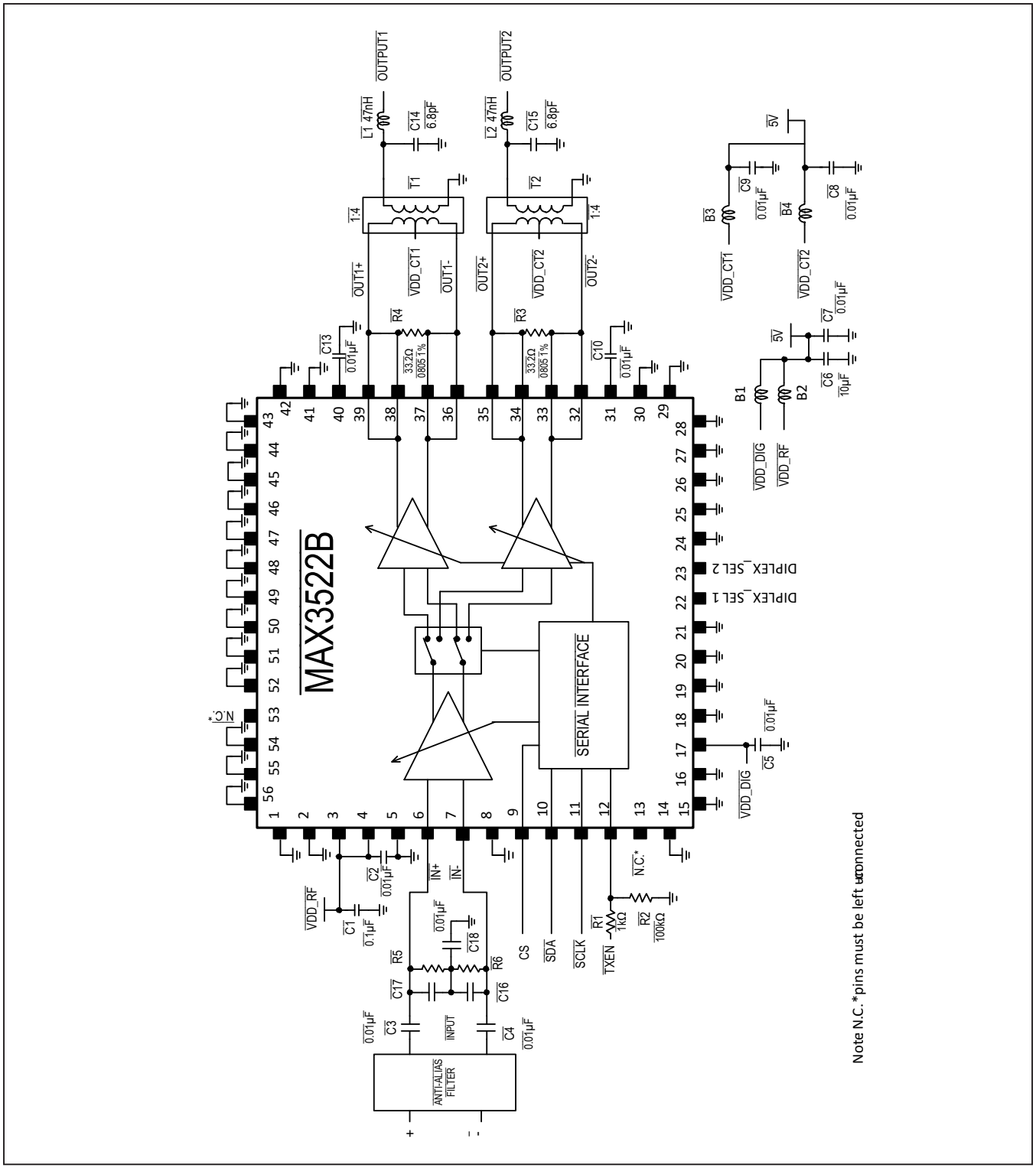
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
3	V_{DD}	+5V Supply. Connect a 0.1µF capacitor to GND.
4	VDD_BYP	Connect a 0.01µF capacitor to GND. Can be shorted to V_{DD}.
6	IN+	Positive input
7	IN-	Negative input
9	CSB	Chip Select. Active-low.
10	SDA	Serial data
11	CLK	Clock
12	TXEN	Transmit enable/disable
13, 53	N.C.	Leave open
31, 40	BYPASS	Connect a 0.01µF capacitor to GND on each BYPASS pin
17	VDD_DIG	Decouple with 0.01µF capacitor to GND, +5V connected on chip.
22	DPLX1	GPIO for diplexer switch control
23	DPLX2	GPIO for diplexer switch control
32, 33	OUT2-	PA2 negative output
34, 35	OUT2+	PA2 positive output
36, 37	OUT1-	PA1 negative output
38, 39	OUT1+	PA1 positive output
1, 2, 5, 8, 14-16, 18-21, 24-30, 41-52, 54-56, Paddle	GND	Ground

Typical Application Circuit



Detailed Description

Programmable-Gain Amplifier

The programmable-gain amplifier (PGA) provides 54dB of output level control in 1dB steps. The gain of the PGA is determined by a 6-bit gain code (GC5–GC0) programmed through the serial-data interface (see Register Map). Specified performance is achieved when the input is driven differentially.

Four power codes (PC1–PC0) allow the PGA to be used with reduced bias current when distortion performance can be relaxed. In addition, for each power code, bias current is automatically reduced with gain code for maximum efficiency.

The PGA features a differential Class A output stage capable of driving an +68dBmV OFDMA signal from 5-85MHz or two 96MHz +65dBmV OFDMA signals from 5-204MHz into a 75Ω load. This architecture provides superior even-order distortion performance but requires that a transformer be used to convert to a single-ended output. In transmit-disable mode, the output amplifiers are powered down, resulting in low output noise while maintaining the impedance match.

3-Wire Serial Programmable Interface (SPI) and Control Registers

The MAX3522B includes three programmable registers for initializing the part and setting the gain and power consumption. The four MSBs are address bits; the eight least significant bits (LSBs) are used for register data. Data is shifted MSB first.

The serial interface should only be written to when TXEN = low, as is the case between transmit bursts in a DOCSIS environment. Once a new set of register data is clocked in, the corresponding power code and/or gain code does not take effect until CS transitions from low to high.

Note: The registers must be written no earlier than 100µs after the device is powered up.

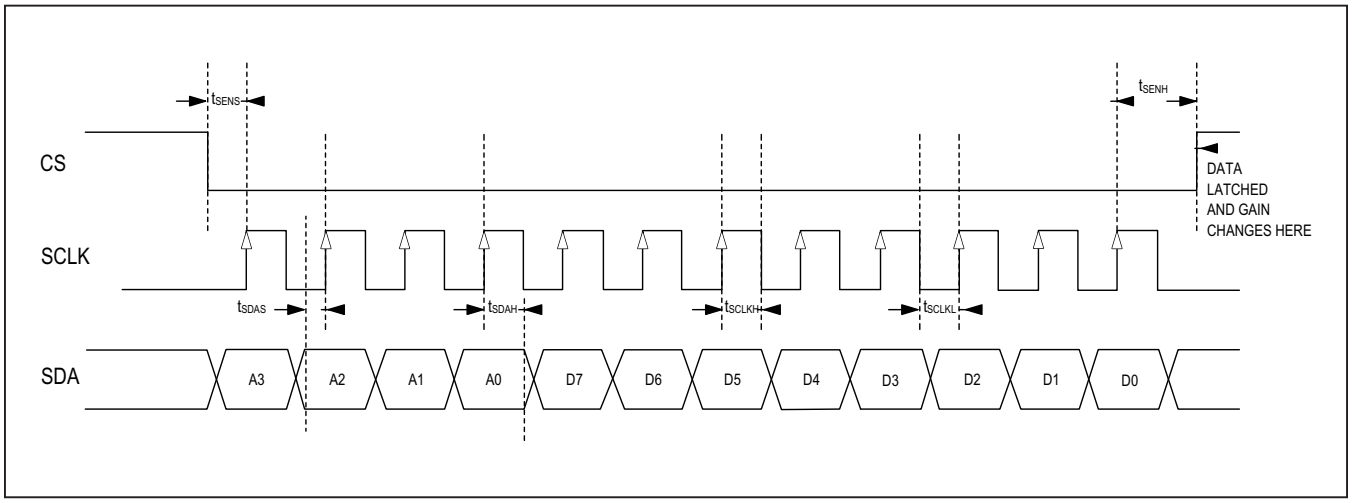


Figure 1: SPI Timing Diagram

Register Map

ADDRESS	NAME	MSB							LSB
Main Registers									
0x00	GAIN[7:0]	PC[1:0]		GC[5:0]					
0x01	CTRL[7:0]	–	–	–	–	–	PASELECT	DPLX2	DPLX1

GAIN (0x00)

BIT	7	6	5	4	3	2	1	0
Field	PC[1:0]		GC[5:0]					
Reset								
Access Type	Write Only		Write Only					

BITFIELD	BITS	DESCRIPTION	DECODE
PC	7:6	Power Control, controls OUTP/OUTN bias current	00: Min 11: Max
GC	5:0	Gain Control	001010: -28dB 111111: +25dB

CTRL (0x01)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	PASELECT	DPLX2	DPLX1
Reset	–	–	–	–	–			
Access Type	–	–	–	–	–	Write Only	Write Only	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
PASELECT	2	Selects which output is used	0: OUT1P/N used, OUT2P/N disabled 1: OUT2P/N used, OUT1P/N disabled
DPLX2	1		0: DPLX2 pin low 1: DPLX2 pin high
DPLX1	0		0: DPLX1 pin low 1: DPLX1 pin high

Applications Information

Power Codes

The device is designed to exceed the stringent linearity requirements of DOCSIS 3.1 using power code (PC) 3. PC = 2, 1, and 0 allow operation at reduced current levels. The full range of gain codes can be used in any power code. The gain difference between power codes is typically less than 0.1dB.

Transmit Disable Mode

Between bursts in a DOCSIS system, the MAX3522B can be put in transmit-disable mode by setting TXEN low. The output transient on the cable is kept well below the DOCSIS 3.1 requirement during the TXEN transitions.

If a gain code or power code change is required, the new values of PC and GC should be clocked in during transmit-disable mode (TXEN low). The new operating point of the MAX3522B is set when $\overline{CS}$ transitions high. This should be performed between transmission bursts.

Initializing the MAX3522B

The MAX3522B includes eight programmable registers for initializing the part and setting gain and power consumption. Each register consists of 4 address bits and eight data bits.On power up, the ROM init bit must be toggled to initialize the internal ROM.

For example, the following sequence initializes the MAX3522B for OUT1 active, not using the GPIO pins:

1) Power up the part with the TXEN pin held low.
2))Write 00h to register 0002 (ROM).
3) Write **08h** to register 0002.
4) Write 00h to register 0002
5) Write 00h to register 0001.
6) Write 00h to register 0002.
7) Write 00h to register 0003.
8) Write 00h to register 0004.
9) Write **06h** to register 0005.
10) Write 00h to register 0006.
11) Write 00h to register 0007.
12) Write the desired values of PC and GC to register 0000

Table 1. Initializing the MAX3522B

REGISTER NAME	REGISTER ADDRESS	MSB BIT LOCATION LSB							
		<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
Power/Gain	0000	PC<1:0>		GC<5:0>					
CTRL	0001	0	0	0	0	0	PASELECT	DPLX<1:0>	
ROM	0002	0	0	0	0	ROM Init	0	0	0
Reg 03	0003	0	0	0	0	0	0	0	0
Reg 04	0004	0	0	0	0	0	0	0	0
Reg 05	0005	0	0	0	0	0	1	1	0
Reg 06	0006	0	0	0	0	0	0	0	0
Reg 07	0007	0	0	0	0	0	0	0	0

PC<1:0> sets the power code, which scales the supply current. Max current is PC = 11, min is PC = 00.

GC<5:0> sets the gain. GC = 111111 corresponds to the maximum voltage gain of 25dB.

PASELECT selects which signal path is used. PASELECT = 0 sets the RF output to pins 36, 37 and 38, 39; PASELECT = 1 sets the RF output to pins 32, 33 and 34, 35.

DPLX<1:0> controls the GPIO pins. DPLX<1> = 0 sets GPIO2 to logic low, DPLX<1> = 1 sets GPIO2 to logic high. DPLX<0> = 0 sets GPIO1 to logic low, DPLX<0> = 1 sets GPIO1 to logic high.

Output Circuit

The output circuit is an open-drain differential amplifier. The outputs should be resistively terminated as shown in the Typical Application Circuit. A 1:4 impedance ratio transformer should be used as the interface between the differential output of the device and the unbalanced 75Ω load.

Amplifier performance depends on the value of the termination resistors. Rated performance is obtained using 33.2Ω termination resistors as shown in the Typical Application Circuit. Increasing the value of this resistor will increase gain and improve SNR at the expense of output return loss.

Transformer core inductance may vary with temperature. Adequate primary inductance must be present to sustain broadband output capability as temperatures vary.

Input Circuit

The differential input impedance of the MAX3522B is 200Ω. In a typical application, however, it is driven from a 100Ω differential source, requiring an external matching resistor. In addition, for rated performance, the common mode impedance of the input must be terminated appropriately. The input network shown in the Typical Application Circuit, C16–C18, R5, and R6, provides this function.

The two 100Ω resistors, R5 and R6, in parallel with the MAX3522B 200Ω input resistance, provide a match for the 100Ω source impedance. The two 5.6pf capacitors, C16 and C17, provide a low-impedance common mode termination out of band. The values of C16 and C17 can be absorbed into an anti-alias filter if one is used.

The device has sufficient gain and linearity to produce an output level of +68dBmV when driven with a +43dBmV input signal. If an input level greater than +43dBmV is used, the 3rd-order distortion performance degrades slightly.

Layout Issues

A well-designed printed circuit board (PCB) is an essential part of an RF circuit. For best performance, pay attention to power-supply layout issues as well as the output circuit layout. The MAX3522B EV board layout can be utilized as a guide during PCB design. Its electrical performance has been thoroughly tested, making it an excellent reference. Refer to the MAX3522B EV kit documentation for additional information.

No Connect Pins

Pins 13 and 53 must be left open, not connected to supply or ground or any other node in the circuit.

Output Circuit Layout

The differential impedance presented to the output pins of the MAX3522B by the 1:4 transformer and the back termination resistor is low, typically less than 15Ω. This means that any series inductance between the part and the transformer will significantly degrade the performance at the higher end of the operating frequency range. Keep the length of the output traces as short as possible. To maintain the balance of the output network, match the length of the differential traces as closely as possible.

Power-Supply Layout

For minimal coupling between different sections of the IC, the ideal power-supply layout is a star configuration. This configuration has a large-value decoupling capacitor at the central power-supply node. The power-supply traces branch out from this node, each going to a separate power-supply node in the circuit. At the end of each of these traces is a decoupling capacitor that provides a very low impedance at the frequency of interest. This arrangement provides local power-supply decoupling at each power-supply pin. The power-supply traces must be capable of carrying the maximum current without significant voltage drop.

The output transformer center tap node (VCC_CT) must be connected to the supply through a ferrite bead. Connect a decoupling capacitor between the center tap and GND.

Exposed Pad Thermal Considerations

The exposed pad (EP) of the MAX3522B's 56-pin TQFN package provides a low thermal resistance path to the die. It is important that the PCB on which the device is mounted be designed to conduct heat from this contact. In addition, the EP should be provided with a low-inductance path to electrical ground. The MAX3522B EV board is an example of a layout that provides optimal thermal and electrical performance.

It is recommended that the EP be soldered to a ground plane on the PCB, either directly or through an array of plated via holes.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX3522BCTN+	0°C to +70°C	56L TQFN-EP*
MAX3522BCTN+T	0°C to +70°C	56L TQFN-EP*

** EP = Exposed pad.*
+ Denotes a lead(Pb)-free/RoHS-compliant package.
T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/17	Initial release	—

