ON Semiconductor®



Initial Product/Process Change Notification Document # : IPCN22170Z

Issue Date: 28 February 2018

Title of Change:	Re-design by metal tune of NCV7425DW0(R2)G and NCV7425DW5(R2)G to correct a design marginality			
Proposed Changed Material First Ship Date:	28 March 2019 or upon customer approval			
Current Material Last Order Date:	30 April 2018 Orders received after the Current Material Last Order Date expiration are to be considered as orders for new changed material as described in this PCN. Orders for current (unchanged) material after this date will be per mutual agreement and current material inventory availability.			
Current Material Last Delivery Date:	28 March 2019 or upon customer approval The Current Material Last Delivery Date may be subject to change based on build and depletion of the current (unchanged) material inventory.			
Product Category:	Active components – Integrated circuits			
Contact information:	Contact your local ON Semiconductor Sales Office or <jean-jacques.goubet@onsemi.com></jean-jacques.goubet@onsemi.com>			
Samples:	Contact your local ON Semiconductor Sales Office to place sample order. Sample requests are to be submitted no later than 45 days after publication of this change notification.			
Sample Availability Date:	31 May 2018			
PPAP Availability Date:	10 August 2018			
Additional Reliability Data:	Contact your local ON Semiconductor Sales Office or <jean-jacques.goubet@onsemi.com>.</jean-jacques.goubet@onsemi.com>			
Type of Notification:	This is an Initial Product/Process Change Notification (IPCN) sent to customers. IPCNs are issued at least 30 days prior to the issuance of the Final Change Notice (FPCN). An IPCN is an advance notification about an upcoming change and contains general information regarding the change details and devices affected. It also contains the preliminary reliability qualification plan. The completed qualification and characterization data will be included in the Final Product/Process Change Notification (FPCN). This IPCN notification will be followed by a Final Product/Process Change Notification (FPCN) at least 12 months prior to implementation of the change. In case of questions, contact <pcn.support@onsemi.com>.</pcn.support@onsemi.com>			
Change Category	Type of Change			
Design	Design Change in Routing			

Description and Purpose:

The main change for the two OPN's NCV7425DW0(R2)G and NCV7425DW5(R2)G is a re-design in the digital core (via metal tune only) to correct a design marginality that could lead to a racing condition for some specific LIN and EN signal transitions and timings. This racing condition may lead to a deadlock situation where it is not possible to wake-up the IC anymore. It only occurs in very specific conditions that may not occur in some types of customer applications.

The opportunity of the re-design was used to implement some other quality improvements in order to better comply with more recent internal ON-Semicondutor requirements:

- Implementation of ring bond pads in place of stacked bond pads (improved bonding reliability)
- Replacement of single via's by double via's when this was possible without re-routing (layout for quality improvements)
- Updated metal 3 level spacings around the MIM capacitor to comply with the latest antenna rules (layout for quality improvements)

The layers that are changed are: metal 1, via 1, metal 2, via 2, metal 3, nitride and polyimide layers.



Initial Product/Process Change Notification Document # : IPCN22170Z Issue Date: 28 February 2018

Reason / Motivation for Change:	 <u>- Change benefits for customer:</u> The re-design version will guarantee that the IC can be waken-up in any conditions thus be functional as expected under all LIN and EN signal transitions and timings circumstances. <u>- Risk for late release for customer:</u> Based on previous experience with similar changes and quality improvements implemented at layout level, the risk of qualification failure and delay in the release is assessed to be very low. The efficiency of the re-design to fix the racing condition has been checked by FIB modification on current parts. So the risk that the re-design would not fix the design marginality is negligible. <u>- Quality improvement:</u> ring bond pads, double via's and metal 3 layer spacing's updates are implemented and are expected to bring manufacturability and quality improvements. 				
Anticipated impact on fit, form, function, reliability, product safety or manufacturability:	The device has been qualified and validated based on the same Product Specification. The device has successfully passed the qualification tests. Potential impacts can be identified, but due to testing performed by ON Semiconductor in relation to the PCN, associated risks are verified and excluded. No anticipated impacts.				
Sites Affected:	ON Semiconductor Sites: ON Oudenaarde, Belgium	iconductor Sites: External Foundry/Subcon Sites:			
Marking of Parts/ Traceability of Change:	From the moment the new re-designed versions are qualified and released to production, they will replace the current variants. The same OPN's will be used. The affected parts will be identified with date codes that ensure product traceability.				
)C619 W0{R2}G and NCV7425DW5{R2}G)				
(NCV7425D PACKAGE: SOIC-16-EP The following qualification will b	W0{R2}G and NCV7425DW5{R2}G) be performed on the re-designed version		ndition	Interval	
(NCV7425D PACKAGE: SOIC-16-EP The following qualification will b Test	W0{R2}G and NCV7425DW5{R2}G) be performed on the re-designed version Specification	Co	ndition	Interval N/A	
(NCV7425D PACKAGE: SOIC-16-EP The following qualification will b	W0{R2}G and NCV7425DW5{R2}G) be performed on the re-designed version		d	Interval N/A N/A	
(NCV7425D PACKAGE: SOIC-16-EP The following qualification will b Test ESD	W0{R2}G and NCV7425DW5{R2}G) be performed on the re-designed version Specification MIL-STD-883	Per standar Per standar • Electrical tests 130degC, 25 de	d d at 3 temperatures: egC and -40 degC 200 samples from C618	N/A	
(NCV7425D PACKAGE: SOIC-16-EP The following qualification will b Test ESD LU Electrical distributions	W0{R2}G and NCV7425DW5{R2}G) be performed on the re-designed version Specification MIL-STD-883 JEDEC standard EIA/JESD78	Per standar Per standar Electrical tests 130degC, 25 dd Sample size: >2 + >200 sample	d d at 3 temperatures: egC and -40 degC 200 samples from C618	N/A N/A	
(NCV7425D PACKAGE: SOIC-16-EP The following qualification will b Test ESD LU Electrical distributions	W0{R2}G and NCV7425DW5{R2}G) be performed on the re-designed version Specification MIL-STD-883 JEDEC standard EIA/JESD78 AEC-Q100-009 lan is expected to be completed on July	Per standar Per standar Electrical tests 130degC, 25 dd Sample size: >2 + >200 sample	d d at 3 temperatures: egC and -40 degC 200 samples from C618	N/A N/A	
(NCV7425D) PACKAGE: SOIC-16-EP The following qualification will b Test ESD LU Electrical distributions The qualification as per above p Electrical Characteristic Sum	W0{R2}G and NCV7425DW5{R2}G) be performed on the re-designed version Specification MIL-STD-883 JEDEC standard EIA/JESD78 AEC-Q100-009 lan is expected to be completed on July	Co Per standar Per standar Electrical tests 130degC, 25 do Sample size: >2 + >200 sample 6 th , 2018.	d d at 3 temperatures: egC and -40 degC 200 samples from C618 s from C619.	N/A N/A	
(NCV7425D) PACKAGE: SOIC-16-EP The following qualification will b Test ESD LU Electrical distributions The qualification as per above p Electrical Characteristic Sum	W0{R2}G and NCV7425DW5{R2}G) e performed on the re-designed version	Co Per standar Per standar Electrical tests 130degC, 25 do Sample size: >2 + >200 sample 6 th , 2018.	d d at 3 temperatures: egC and -40 degC 200 samples from C618 s from C619.	N/A N/A	
(NCV7425D) PACKAGE: SOIC-16-EP The following qualification will b Test ESD LU Electrical distributions The qualification as per above p Electrical Characteristic Sum Electrical characteristics are not	W0{R2}G and NCV7425DW5{R2}G) The performed on the re-designed version	Co Per standar Per standar Electrical tests 130degC, 25 de Sample size: >2 + >200 sample 6 th , 2018.	d d at 3 temperatures: egC and -40 degC 200 samples from C618 s from C619. CN.	N/A N/A	
(NCV7425D) PACKAGE: SOIC-16-EP The following qualification will b Test ESD LU Electrical distributions The qualification as per above p Electrical Characteristic Sum Electrical characteristics are not List of Affected Standard Pa	W0{R2}G and NCV7425DW5{R2}G) The performed on the re-designed version	Co Per standar Per standar Electrical tests 130degC, 25 de Sample size: >2 + >200 sample 6 th , 2018.	d d at 3 temperatures: egC and -40 degC 200 samples from C618 s from C619. CN.	N/A N/A N/A	
(NCV7425D) PACKAGE: SOIC-16-EP The following qualification will b Test ESD LU Electrical distributions The qualification as per above p Electrical Characteristic Sum Electrical characteristics are not List of Affected Standard Par Current Part Number	W0{R2}G and NCV7425DW5{R2}G) The performed on the re-designed version	Co Per standar Per standar Electrical tests 130degC, 25 de Sample size: >2 + >200 sample 6 th , 2018.	d d at 3 temperatures: egC and -40 degC 200 samples from C618 s from C619. CN. Qualific NCV7	N/A N/A N/A	
(NCV7425D) PACKAGE: SOIC-16-EP The following qualification will b Test ESD LU Electrical distributions The qualification as per above p Electrical Characteristic Sum Electrical characteristics are not List of Affected Standard Pai Current Part Number NCV7425DW0G	W0{R2}G and NCV7425DW5{R2}G) The performed on the re-designed version	Co Per standar Per standar Electrical tests 130degC, 25 de Sample size: >2 + >200 sample 6 th , 2018.	d d d at 3 temperatures: egC and -40 degC 200 samples from C618 s from C619. CN. Qualific NCV7 NCV74	N/A N/A N/A ation Vehicle	

Appendix A: Changed Products

Product	Customer Part Number	New Part Number	Qualification Vehicle
NCV7425DW0R2G		NA	NCV7425DW0R2G
NCV7425DW5R2G		NA	NCV7425DW5R2G