

XIO3130 PCI Express Packet Switch Silicon Errata

- Setting the secondary bus reset on the host chipset or on the upstream bridge of the switch will cause an 80-100ns reset pulse on the secondary bridge (PG2.0, PG2.1)

Description	The same thing is observed regardless if the DNx_DPSTRP terminal is high or low. Setting the secondary bus reset on an upstream bridge should only cause a hot reset on the bus to which the the reset is being applied. It should not cause a fundamental reset on bridges that are downstream.
Impact	Low
Workaround	None

- When operating in normal mode, the downstream resets (DNx_PERST#) will de-assert before the downstream reference clock is stable (PG2.0, PG2.1)

Description	DNxPERST# should de-assert 100us after DNx_REFCLK is valid, but instead DNx_PERST# is de-asserting just as DNx_REFCLK is starting. This can cause downstream devices to fail if the devices requires a clock before the reset is de-asserted.
Impact	High
Workaround	The problem can be avoided by operating the device in Hot Plug mode. In this mode, the DNx_PERST# will deassert approximately 100ms after UP_PERST# de-assert which allows enough time for the downstream reference clock to stabilize.

- Enabling ASPM L0s or L1 on the switch may cause the switch to malfunction.

Description	Some problems have been identified when the XIO3130 is placed into the L0s or L1 ASPM state resulting in loss of TLP traffic on the link. The problem occurs when both upstream and any of the downstream ports have L0s and/or L1 enabled.
Impact	It has been observed that TLPs may not traverse through the switch when both the upstream and one, two or all downstream ports have L0s and/or L1 enabled.
Workaround	Do not enable ASPM L0s or L1 in the XIO3130.

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